Matrox Helios

Installation and Hardware Reference

Manual no. 10879-101-0210

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Chapter 1

Introduction

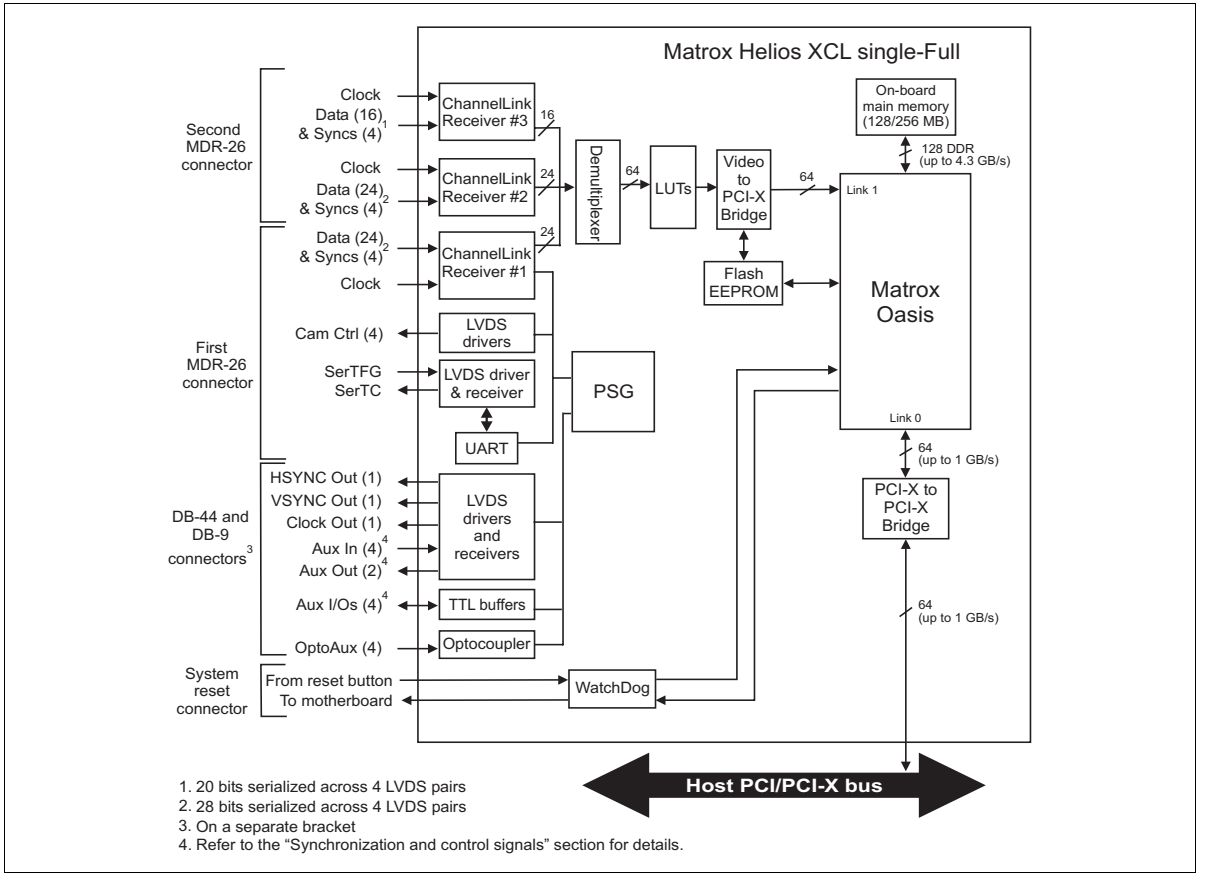
This chapter briefly describes the features of the Matrox Helios board, as well as the software that can be used with the board.

Matrox Helios boards

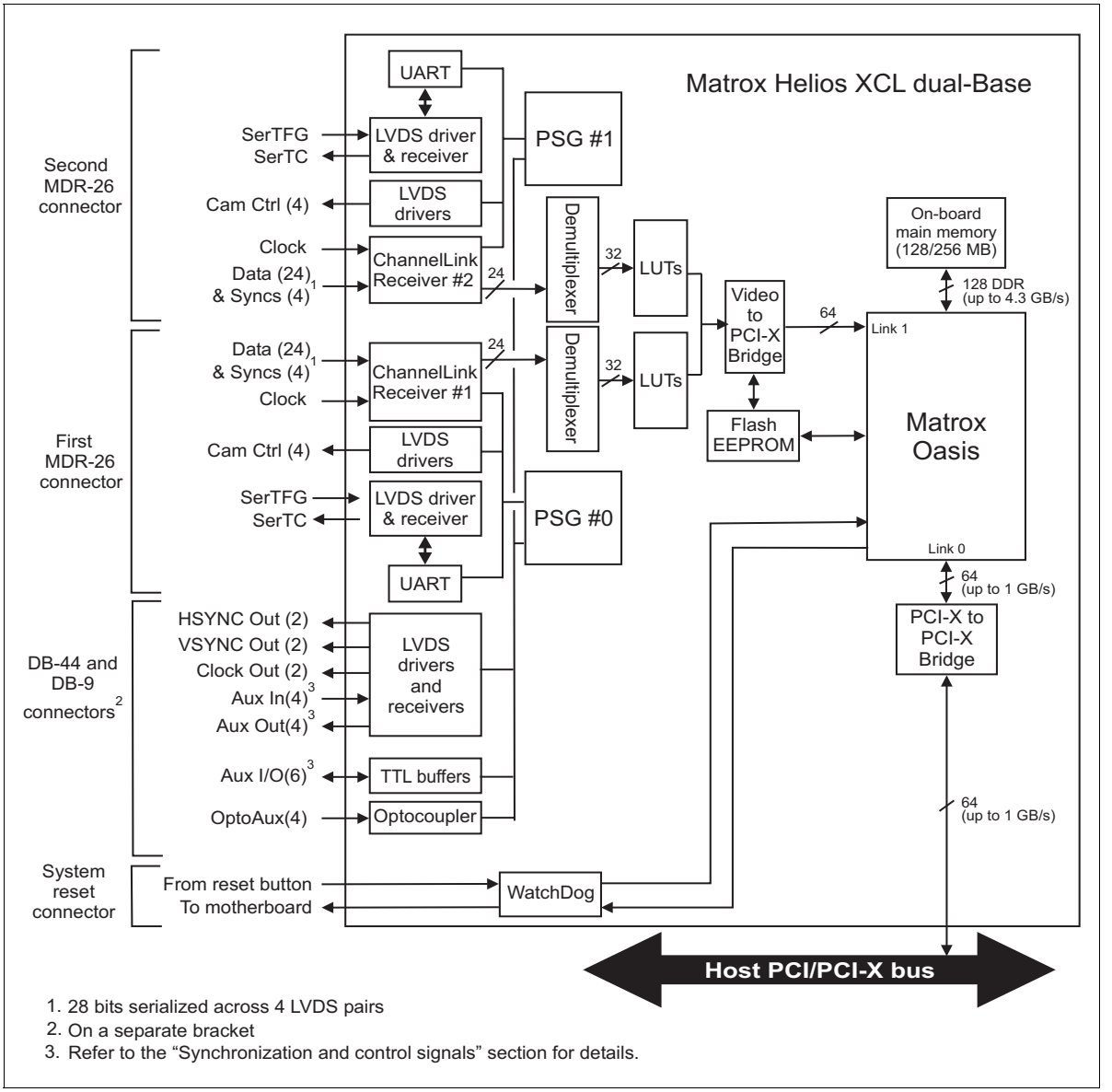
The Matrox Helios family consists of three PCI-X compliant, single-slot, frame grabbers with powerful preprocessing capabilities: Matrox Helios XCL, Matrox Helios XA, and Matrox Helios XD.

Acquisition with Matrox Helios XCL

Matrox Helios XCL is a high-performance Camera Link frame grabber. It is available in two factory-configured versions: a dual-Base version and a single-Full version. The dual-Base version supports simultaneous acquisition from two completely independent Camera Link video sources utilizing the Base configuration. The single-Full version supports acquisition from a single Camera Link video source utilizing the Base, Medium, or Full configuration. Both versions can operate at full Camera Link speed.



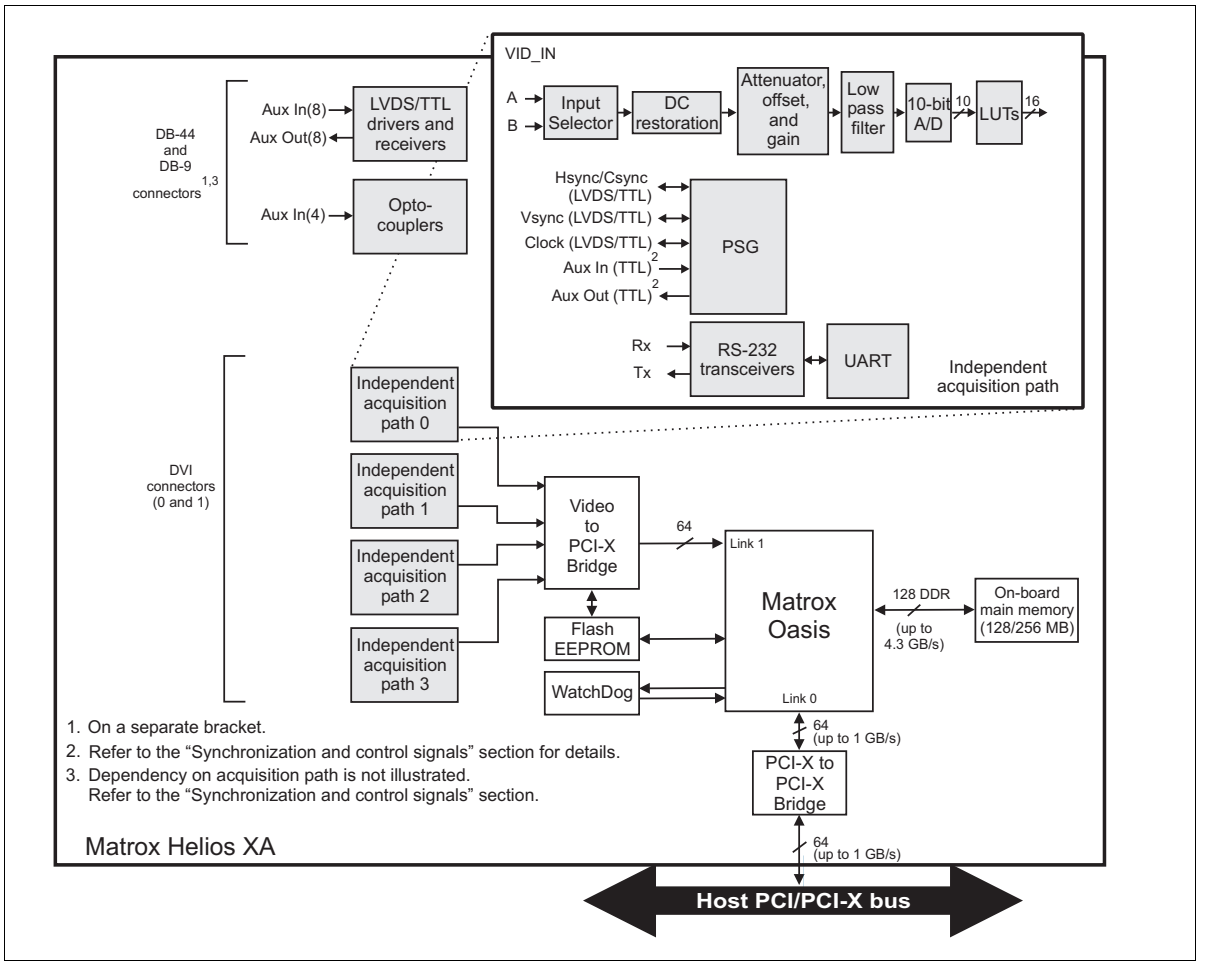
1. 20 bits serialized across 4 LVDS pairs
2. 28 bits serialized across 4 LVDS pairs
3. On a separate bracket
4. Refer to the “Synchronization and control signals” section for details.



1. 28 bits serialized across 4 LVDS pairs
2. On a separate bracket
3. Refer to the “Synchronization and control signals” section for details.

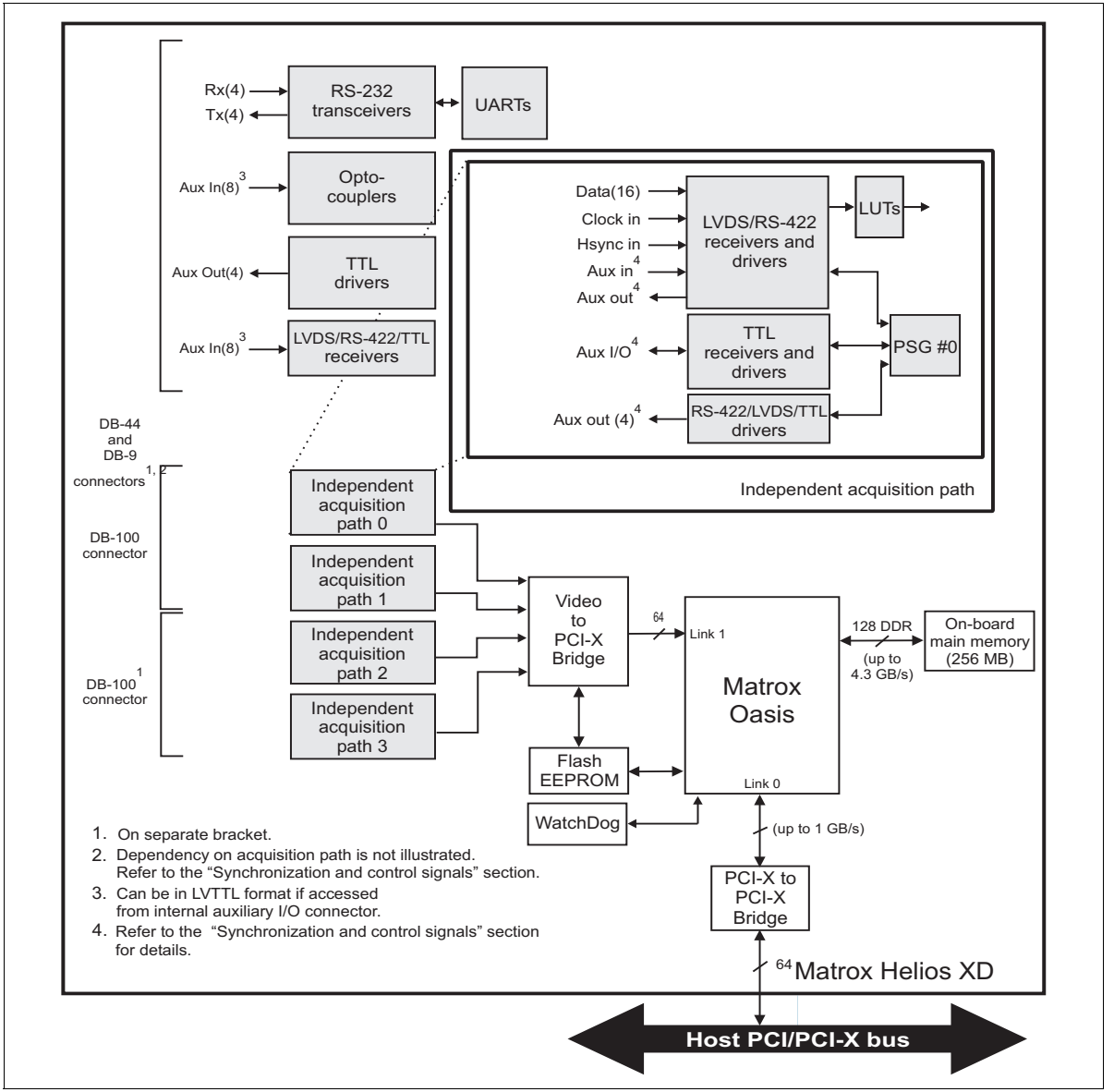
Acquisition with Matrox Helios XA

Matrox Helios XA is a high-performance analog frame grabber, capable of high frequency and high fidelity simultaneous acquisition from up to four independant video sources. For added flexibility, each acquisition path has an input selector that can switch between receiving input from one of two video sources. This means, for example, you can connect two 4-tap video sources and switch between them.



Acquisition with Matrox Helios XD

Matrox Helios XD is a high-performance digital frame grabber, capable of image acquisition across four synchronous or asynchronous digital channels. Each channel is 16-bits wide and can capture video from LVDS or RS-422 digital video sources, depending on the version of Matrox Helios XD purchased.



Processing capabilities

To alleviate the image formatting and preprocessing tasks performed by the CPU of the host computer (Host), all Matrox Helios boards include the custom Matrox Oasis ASIC. Using this ASIC, Matrox Helios can preprocess and format grabbed data before transferring it to the Host.

❖ Although the Host can also transfer images to Matrox Helios and use Matrox Oasis to perform some time consuming, supported processing operations, this is typically not recommended. You can lose efficiency and performance by transferring the data back and forth between the Host and Matrox Helios.

Matrox Oasis

Matrox Oasis is a high-density chip that integrates the pixel accelerator (PA), a links controller with data formatters, and main memory controller.

PA

The PA is a parallel processing core, which considerably accelerates neighborhood, point-to-point, and LUT mapping operations. The PA can perform up to 80 billion operations per second. In addition, I/O-bound functions, such as image arithmetic functions, benefit from the 4.3 Gbytes/sec memory bandwidth of Matrox Oasis.

The PA consists of an array of 64 processing elements, all working in parallel. Each processing element has a multiply-accumulate (MAC) unit and an arithmetic-logic unit (ALU). The MAC unit is capable of performing a single 16-bit by 16-bit, two 8-bit by 16-bit, or four 8-bit by 8-bit multiplies with 40-bit accumulation per cycle for convolution operations. The ALU can execute a wide variety of arithmetic and logical operations, and can be programmed to execute a sequence of 256 instructions per pixel at one instruction per cycle.

Links Controller

The links controller (LINX) is the router that manages all data movement within Matrox Helios. It oversees the transfer of image data from the frame grabber section to on-board memory for preprocessing and from on-board memory to Host or display memory. Image data can be subject to various formatting operations, including: plane separation on input and merging on output, input cropping, input and output subsampling (1 to 16), and independent control of horizontal and vertical scanning direction. The latter is particularly useful for reconstructing a proper image from a video source whose readout requires multiple taps, each with different scanning directions.

Memory controller

Matrox Oasis includes a very efficient main memory controller for managing the DDR 128-bit wide interface to on-board main memory (DDR SDRAM). Operating at 133 MHz, the DDR SDRAM memory and controller combine to

deliver a memory bandwidth in excess of 4 Gbytes/sec. This memory bandwidth allows Matrox Helios to comfortably handle demanding video I/O while maintaining PA performance.

Main memory

Matrox Helios supports up to 256 Mbytes of linearly addressable, DDR SDRAM main memory, which is accessed through Matrox Oasis. Main memory holds image and post-processing result data.

Additional functionality

In addition to the core video capture and preprocessing capabilities, Matrox Helios incorporates a variety of features to simplify overall system integration. These features include:

- Auxiliary, multi-purpose signals, that can be programmed for trigger input, field polarity input, timer clock input, user-defined input, exposure output, or user-define output, depending on the signal. Matrox Helios XCL supports up to 18 depending on the version, Matrox Helios XA supports up to 28, and Matrox Helios XD supports 44 auxiliary signals.

- LVDS or RS-232 compatible serial interfaces (number depends on the type and version of Matrox Helios). Each interface is mapped as a COM port so that it can be accessed through the Win32 API. The serial interface can both receive and transmit signals, in full-duplex mode.

- Hardware facilities for implementing custom software-based motion detection.

- An integrated Watchdog timer[1] for automatically recovering from application or system failure.

- An internal video generator for troubleshooting both installation and operation.

1. Starting from revision 1 of the Matrox Helios XCL PCB; whereas, present on the Matrox Helios XA PCB as of revision 0.

- Matrox Helios XA also has a bi-color LED per timing and control section to monitor PLL operation and sychronization signal input.
- Supports an integrated quadrature decoder[1].

Data transfer

Matrox Helios can exchange data with the Host at a peak of up to 1 Gbyte/sec when used in a PCI-X slot. Matrox Helios can also be used in a conventional PCI[2] slot, in which case the maximum transfer rate is reduced (132 Mbytes/sec for a 33 MHz 32-bit PCI slot, 266 Mbytes/sec for a 66 MHz 32-bit PCI slot, 532 Mbytes for a 66 MHz 64-bit PCI slot).

Although the Matrox Helios boards don't have an integrated display section, images can be transferred either to any available Matrox display board or a third-party display board in the computer.

Important

Note that transfer of image data to a display board might require intervention from the Host CPU, depending on your computer's architecture.

Documentation conventions

This manual refers to all Matrox Helios boards as Matrox Helios. When necessary, it distinguishes between them using their full name. Also note that, when the term Host is used in this manual, it refers to the host computer.

Software

To operate Matrox Helios, you can purchase one or more Matrox Imaging software products that supports the board. These are the Matrox Imaging Library (MIL) and its derivatives (MIL-Lite, ActiveMIL, ActiveMIL-Lite, and Matrox Inspector). All Matrox software is supported under Windows; consult your software manual for supported Windows environments.

❖ Note that, although other software products might be available to operate Matrox Helios, the discussion throughout this manual is based in terms of Matrox Imaging software products.

1. Although not documented prior to revision 10879-101-0200 of the manual, a quadrature decoder has been featured in the PSGs of Matrox Helios frame grabbers since the first revision of their PCB.
2. 5 V starting from revision 1 of the Matrox Helios PCB; revision 0 is only 3.3 V PCI tolerant.

MIL

MIL is a high-level programming library with an extensive set of optimized functions for image capture, processing, analysis, transfer, compression, display, and archiving. Image processing operations include point-to-point, statistical, spatial filtering, morphological, geometric transformation, and FFT operations. Analysis operations support calibration, are performed with sub-pixel accuracy, and include pattern recognition (normalized grayscale correlation and Geometric Model Finder), blob analysis, edge extraction and analysis, measurement, optical character recognition (OCR), and code recognition (1D, 2D and composite code types). calibration, optical character recognition (OCR), pattern recognition (normalized grayscale correlation and Geometric Model Finder), edge finding, and code read/write operations.

MIL applications are easily ported to new Matrox hardware platforms and can be designed to take advantage of multi-processing and multi-threading environments.

MIL-Lite

MIL-Lite is a subset of MIL. It includes all the MIL functions for image acquisition, transfer, display control, and archiving.

ActiveMIL

ActiveMIL is a set of ActiveX controls that are based on MIL. ActiveMIL was designed for rapid application development (RAD) tools, such as Microsoft's Visual Basic. ActiveMIL is included with MIL (ActiveMIL-Lite is included with MIL-Lite).

Matrox Inspector

Matrox Inspector is an interactive Windows application for image capture, processing, analysis, and archiving. MIL application developers can use Matrox Inspector as a prototyping tool to quickly build proof-of-concept demonstrations. End users can use Matrox Inspector to perform and automate image enhancement and measurement tasks.

Matrox Intellicam

Matrox Intellicam is an interactive Windows program that allows for fast video source interfacing and provides interactive access to all the acquisition features of your Matrox board. Matrox Intellicam also has the ability to create custom digitizer configuration format (DCF) files, which MIL and its derivatives use to interface to specific non-standard video sources. Matrox Intellicam is included with all Matrox Imaging software products.

Essentials to get started

To begin using Matrox Helios, you must have a computer with the following:

- An available conventional PCI slot[1] or a PCI-X slot.
- Processor with an Intel 32-bit architecture (IA32) or equivalent.
- A relatively up-to-date PCI/PCI-X chipset, such as the Intel E7500 series, AMD-8000 series, ServerWorks (HE, LE, LC, or HE SL), or ServerWorks GC (HE, LE, WS, or SL).

Important

- Proper ventilation. Refer to the *Ventilation requirements* section of *Appendix B: Technical information*.
- Microsoft Windows (consult the software package for specific supported environments and computer memory/storage requirements).
- A CD drive, and a hard disk or network drive on which to install the Matrox Helios software.

Matrox does not guarantee compatibility with all computers that have the above specifications. Please consult with your local Matrox Imaging representative, local Matrox Imaging sales office, or the Matrox Imaging Customer Support Group at headquarters before using a specific computer.

Inspecting the Matrox Helios package

You should check the contents of your Matrox Helios package when you first open it. If something is missing or damaged, contact your Matrox representative.

Standard items

You should receive the following items:

- The Matrox Helios XA, XCL, or XD board, depending on which was ordered. If you purchased a Matrox Helios XD, make sure you have recieved the appropriate version (LVDS or RS-422) of the board.

1. 5 V starting from revision 1 of the Matrox Helios PCB; revision 0 is only 3.3 V PCI tolerant.

- An adapter board, and a flat ribbon cable to interface the frame grabber with the adapter board. Note that the adapter board is specific to the type of Matrox Helios board purchased.

- If you purchased a Matrox Helios XD, you should also receive a digital video input adapter board and corresponding flat ribbon cable.

- A supplementary 50-pin auxiliary I/O mating connector. The mating connector is included in case you need to build a cable that can access the signals of the internal auxiliary I/O connector from within the chassis.

- The *Matrox Helios Installation and Hardware Reference* manual (this document).

Available separately

You might have also ordered one or more of the following:

- MIL, which includes ActiveMIL; MIL-Lite, which includes ActiveMIL-Lite; or Matrox Inspector. Matrox Intellicam is included with each of the aforementioned software packages.

- DVI-TO-8BNC/O, an 8-foot (2.4 m) cable with a DVI connector on one end and both 8 BNCs and open-ended wires on the other end. This cable is meant to connect to Matrox Helios XA. The open-ended wires allow you to connect to the synchronization and control signals of the module.

Important

To connect the output of a display board (with a DVI output connector) to the analog video input connectors, you can use a standard cable (DVI-I to DVI-I or DVI-A to DVI-A cable) if the display board encodes the synchronization signals on the video data (sync on green). Otherwise, you must use the Matrox DVI-TO-8BNC/O cable or a custom cable that re-routes the synchronization signals to the appropriate pins.

❖ If needed, you can purchase a Camera Link cable from the video source manufacturer, 3M Interconnect Solutions for Factory Automation, Intercon 1, or other third parties.

Handling components

The electronic circuits in your computer and the circuits on Matrox Helios are sensitive to static electricity and surges. Improper handling can seriously damage the circuits. Be sure to drain static electricity from your body by touching a metal fixture (or ground) before you touch any electronic component. In addition, do not let your clothing come in contact with the circuit boards or components.

Warning

Before you add or remove devices from your computer, always **turn off** the power to your computer and all peripherals.

Installation

The installation procedure consists of the following steps:

1. Complete the hardware installation procedure described in Chapter 2.
2. Complete the software installation procedure described in the documentation accompanying your software package.

More information

For information on using multiple Matrox Helios boards, refer to Chapter 3.

For in-depth hardware information, refer to Chapter 4; whereas for a summary of this information, as well as environmental and electrical specifications, connector pinout descriptions, and ventilation requirements, see Appendix B.

Need help?

If you experience problems during installation or while using this product, refer to the support page on the Matrox Imaging web site: www.matrox.com/imaging/support. This page provides answers to frequently asked questions, as well as offers registered customers additional ways of obtaining support.

If your question is not addressed and you are registered, you can contact technical support. To do so, you should first complete and submit the online Technical Support Request Form, accessible from the above-mentioned page. Once the information is submitted, a Matrox support agent will contact you shortly thereafter by email or phone, depending on the problem.

Chapter

2

Hardware installation

This chapter explains how to install your Matrox Helios board in your computer.

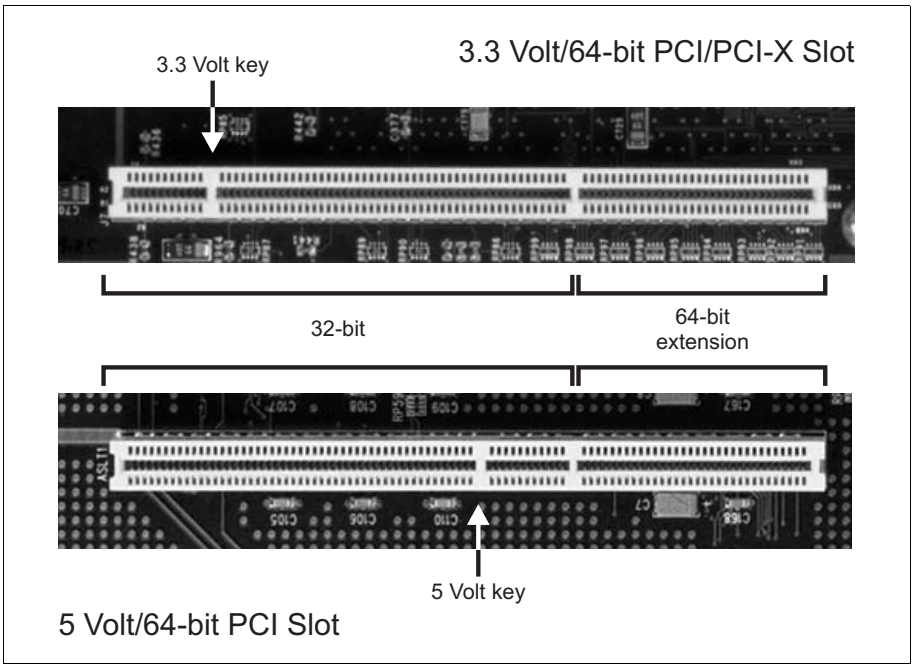
Installing your Matrox Helios board

Before you install your Matrox Helios board, some precautionary measures must be taken. Turn off the power to your computer and its peripherals, and drain static electricity from your body (by touching a metal part of the computer chassis).

Proceed with the following steps to install your board. Note that your board should be installed before you install your software.

1. Remove the cover from your computer; refer to your computer's documentation for instructions.

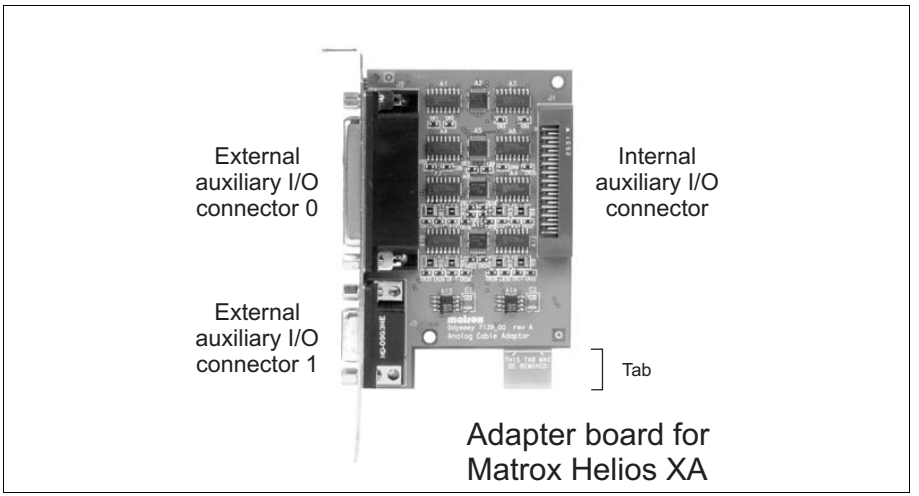
2. Check that you have an empty PCI-X slot in which to install your Matrox Helios XCL, XA, or XD board. It can also be installed in a conventional 32- or 64-bit PCI[1] slot, but this will reduce the transfer rate between the board and the Host. For the Matrox Helios XA and XD boards, the slot must be able to accomodate a full-length board.



Important

Some computers have a large, black-ridged heat sink that prevents long boards from using some of the PCI board slots. Matrox Helios ***must not*** touch the heat sink. Therefore, choose a slot where the board completely avoids it. If you cannot find a suitable slot, contact your computer dealer.

If you also need to install the adapter board(s) of Matrox Helios XCL, XA, or XD, you need an additional slot. This slot need not be adjacent to the Matrox Helios XCL, XA or XD board. Note that the adapter boards do not plug into a slot's PCI/PCI-X connector; they attach only to the back of the computer's chassis. Since the Matrox Helios XA's adapter board is longer, it has a support tab that can be removed; if a PCI/PCI-X slot is selected, the tab will fit into the slot's connector, ensuring that the board does not move



If necessary, remove boards from your computer to make room for your Matrox Helios board and if required, its adapter board.

3. If there is a metal plate at the back of the selected slots, remove it. Keep the screw from the top of the plates to anchor your boards once they are installed.

4. If Watchdog functionality[1] is required, install the appropriate cables as described in *Installing the cables for Watchdog functionality* section, later in this chapter.

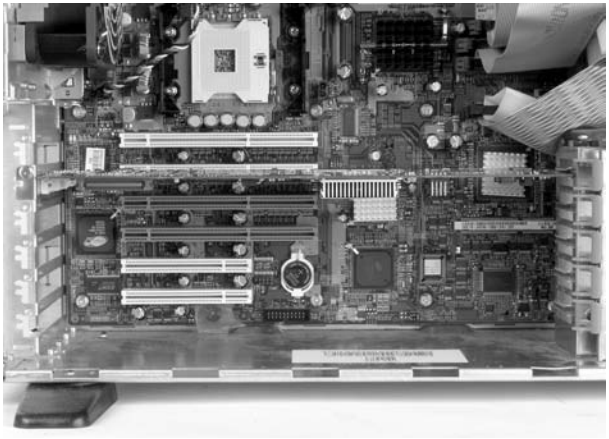
1. 5 V starting from revision 1 of the Matrox Helios PCB; revision 0 is only 3.3 V PCI tolerant.

5. Position your Matrox Helios XCL, XA or XD board in the selected slot, and then press the board firmly but carefully into the connector of the slot.

   When installing Matrox Helios in a conventional 32-bit slot, only the 32-bit portion of the edge connector is connected in the slot. The other portion will remain out.

   Note that Matrox Helios XA has a PCI board retainer attached to it. This is because some computers have both PCI/PCI-X and longer slots (for example, ISA or EISA slots). In such computers, the shorter PCI/PCI-X board needs a retainer to slide between the guides and hold it firmly in place. If your computer has only PCI/PCI-X slots, unscrew the PCI board retainer from the Matrox Helios board.

6. Anchor the board using the screw that you removed in step 3



7. When installing a Matrox Helios XD, install the digital video adapter board, if required, as described in the section *Installing the digital video adapter board*, later in this chapter.

1. Starting from revision 1 of the Matrox Helios XCL PCB; whereas, present on the Matrox Helios XA PCB as of revision 0.

8. If required, install the adapter board of your Matrox Helios board, as described in the section *Installing an adapter board*, later in this chapter.

9. Turn on your computer.

❖ Under Windows 2000/XP, when you boot your computer, Windows' Plug-and-Play system will detect a new Multimedia Video Device and you will be asked to assign it a driver. At this point, you should click on **Cancel** because the driver will be installed during the installation of Matrox Helios software.

Installing the cables for Watchdog functionality

If Watchdog functionality[1] is required:

1. Create a custom cable (Cable A) with a standard, 0.1" spacing, 2-pin female connector at one end, and at the other end, a connector that fits into the Reset button connector of the chassis (see the subsection *System reset connector* of the section for the required board in *Technical information*).

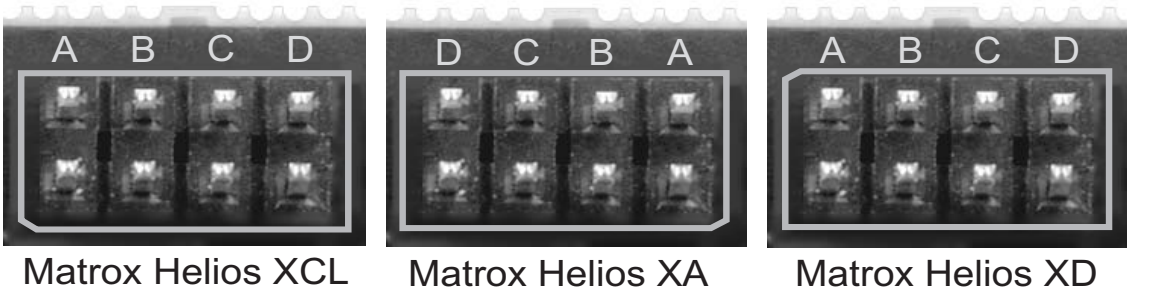
2. Create a second custom cable (Cable B) with a standard, 0.1" spacing, 2-pin female connector at one end, and at the other end, a connector that fits into the motherboard reset connector (see the above-mentioned subsection).

3. Disconnect the end of the Reset button cable currently attached to the Reset button connector of the chassis, and attach Cable A to this connector instead.

4. Disconnect the end of the the Reset button cable currently attached to your motherboard reset connector, and attach Cable B to this connector instead.

1. Starting from revision 1 of the Matrox Helios XCL PCB; whereas, present on the Matrox Helios XA PCB as of revision 0.

5. Connect Cable A to the B pin-pair of the system reset connector of Matrox Helios



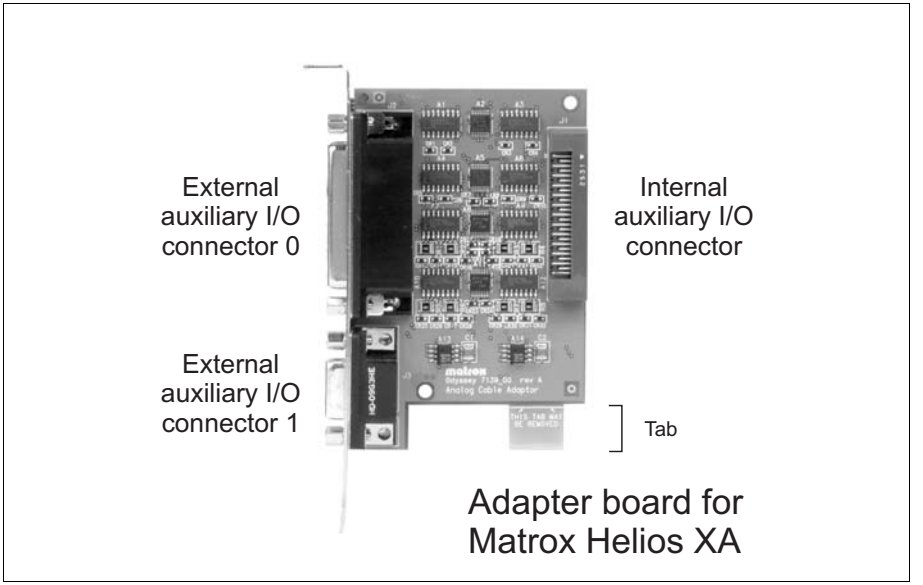
6. Connect Cable B to the A pin-pair of the system reset connector of the Matrox Helios.

Installing an adapter board

To install the adapter board of Matrox Helios XCL, XA, or XD, proceed with the following steps.

1. Make sure that your Matrox Helios XCL, XA, or XD board is fastened to the computer chassis.

2. If you are installing the adapter board of Matrox Helios XA and the slot that you have selected for the board is not a PCI/PCI-X slot, break off the board's tab if it interferes with other components in the computer. The tab was added so that if used in a PCI/PCI-X slot, the board would have extra support and be more sturdy.

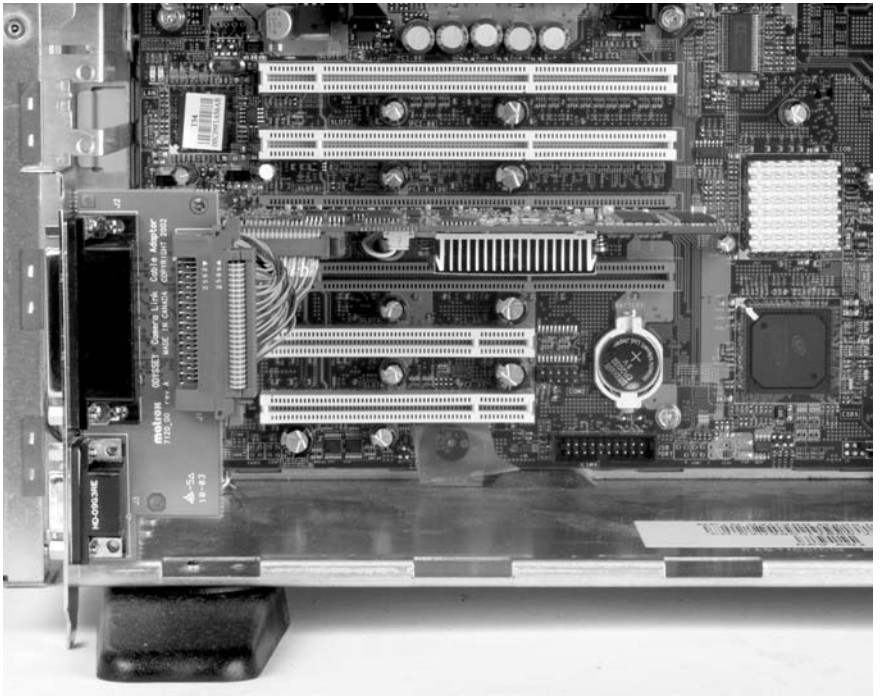


   To break off the tab, use a set of pliers; there is a groove along the tab so that you can break it off without an excessive amount of force.

3. Connect the adapter board's flat ribbon cable to the internal auxiliary I/O connector of the Matrox Helios board. To do so, position the cable so that the red wire is on the same side as the bracket of the Matrox Helios board. With the Matrox Helios board and the cable in this position, only the connector on one end of the cable will latch properly onto the internal auxiliary I/O connector. The other end will not and excessive force might damage the cable connector.

   In addition, you should hear a snap when the hooks of the cable's connector latch onto the internal auxiliary I/O connector.

4. Connect the other end of the flat ribbon cable to the internal auxiliary I/O connector of the adapter board. Position the connectors so that their triangular etchings face each other. The etchings indicate the location of pin 1.



5. If you are installing the adapter board of Matrox Helios XA in a PCI/PCI-X slot, align the board's tab with the slot's connector, and then press the board firmly but carefully into the slot's connector. For other types of slots or when installing the adapter board of Matrox Helios XCL, slide the board's bracket into the opening at the back of the selected slot.

6. Anchor the adapter board's bracket to the chassis using the screw that you removed in the previous section.

Installing the digital video adapter board

To install the digital video adapter board:

1. Make sure that your Matrox Helios XD board is fastened to the computer chassis.

2. Then, connect the flat ribbon cable to the internal digital video input connector of the Matrox Helios frame grabber. To do so, position the cable so that red wire is on the same side as the bracket of the Matrox Helios XD board.

   With the Matrox Helios board and the cable in this position, only the connector on one end of the cable will latch properly onto the internal digital video input connector. The other end will not and excessive force might damage the cable connector.

   In addition, you should hear a snap when the hooks of the cable's connector latch onto the internal digital video input connector.

3. Connect the other end of the flat ribbon cable to the internal digital video input connector of the adapter board. Position the connectors so that their triangular etchings face each other. The etchings indicate the location of pin 1.

4. Slide the adapter board's bracket into the opening at the back of the selected slot.

5. Anchor the adapter board's bracket to the chassis using the screw that you removed in the first section.

Connecting video sources

Connecting to Matrox Helios XCL

The Matrox Helios XCL board has the following connectors:

- **Two Camera Link-compliant video input connectors (on the bracket).** Used to receive video input, timing, and synchronization signals and transmit/receive communication signals between the video source and the frame grabber.

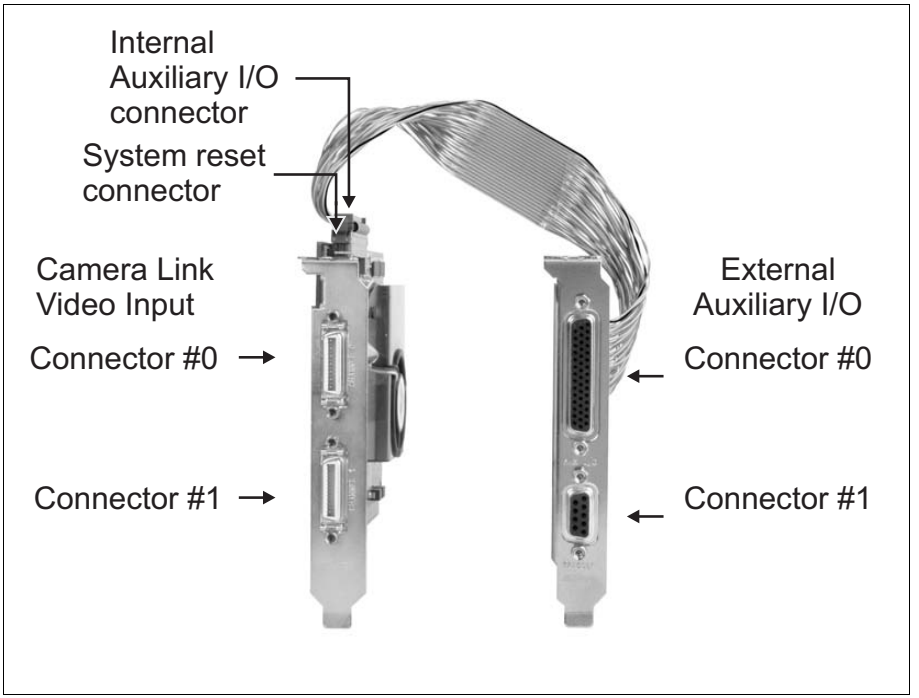
- **Internal auxiliary I/O connector (50-pin).** Used to transmit timing and synchronization signals, and transmit/receive auxiliary signals. The connector is located on the edge of the board, making the signals accessible from inside the computer enclosure.

- **System reset connector.** Used to reset the motherboard if the reset button is pressed or the Watchdog circuitry of Matrox Helios detects abnormal Host inactivity.

To access the signals of the internal auxiliary I/O connector from outside of the computer enclosure, you might have installed the corresponding adapter board. It has the following connectors:

- **External auxiliary I/O connector 0 (HD-44).** Used to transmit timing and synchronization signals, and transmit/receive auxiliary signals.

- **External auxiliary I/O connector 1 (DB-9).** Used to transmit/receive auxiliary signals.



Depending on if you are using the single-Full or dual-Base version of Matrox Helios XCL, you can connect one or two video sources to the pair of Camera Link connectors, respectively. Use standard Camera Link cables. You can purchase such a cable from your video source manufacturer, 3M Interconnect Solutions for Factory Automation, Intercon 1, or other third parties. Note that this cable is not available from Matrox. If using both Camera Link connectors on the single-Full version of the board, the cables must be of the same type and length.

Connecting to Matrox Helios XA

The Matrox Helios XA board has the following connectors:

- **Two DVI analog video input connectors (on the bracket).** Used to receive video input signals and transmit/receive timing, synchronization, and communication signals between the video source and the frame grabber. To each connector, you can connect up to 4 video sources. Connector 0 provides source A for acquisition paths 0 through 3, and Connector 1 provides source B for acquisition paths 0 through 3.

- **Internal auxiliary I/O connector (50-pin).** Used to transmit/receive the auxiliary, camera control, timing, and synchronization signals in TTL format. The connector is located on the edge of the board, making the signals accessible from inside the computer enclosure.

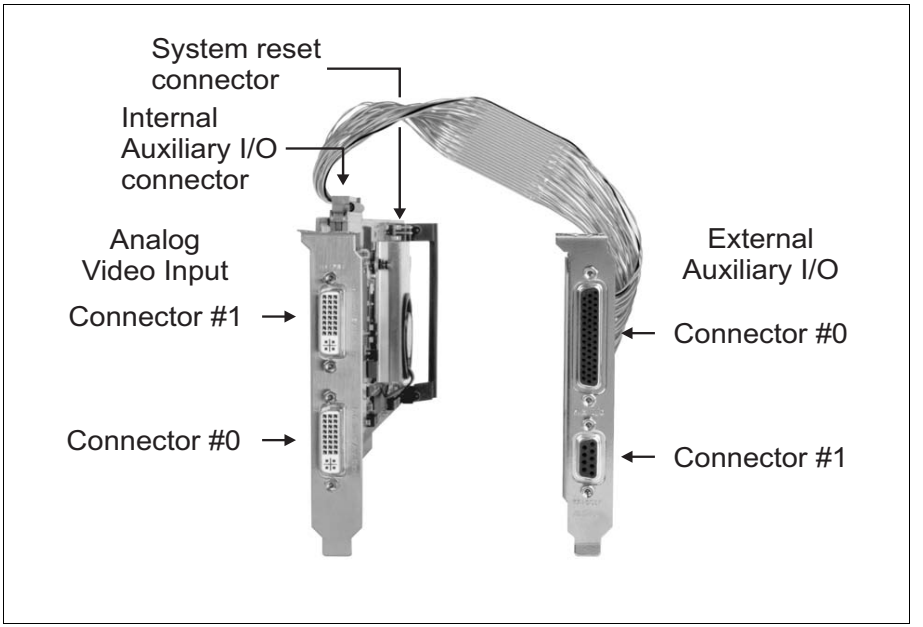
- **System reset connector**[1]**.** Used to reset the motherboard if the reset button is pressed or the Watchdog circuitry of Matrox Helios detects abnormal Host inactivity.

To access the signals of the internal auxiliary I/O connector from outside of the computer enclosure, you might have installed the corresponding adapter board. It has the following connectors:

- **External auxiliary I/O connector 0 (HB-44).** Used to transmit/receive synchronization and auxiliary signals. Note that all the signals can be in either LVDS or TTL format.

- **External auxiliary I/O connector 1 (DB-9).** Used to receive opto-isolated trigger input signals.

1. Starting from revision 1 of the Matrox Helios XCL PCB.



You can use the Matrox DVI-TO-8BNC/O cable to connect to your video sources. The cable has a DVI connector on one end and both 8 BNCs and open-ended wires on the other end; the open-ended wires allow you to connect to some timing, synchronization, and control signals of the frame grabber. Two of these cables are required to connect to more than 4 video sources.

Connect the cable's DVI connector to one of the DVI connectors on Matrox Helios XA. Then, connect the BNC connectors as follows.

BNC label	Signal on DVI connector 0	Signal on DVI connector 1	Expected input, with respect to the DVI connector.
VID IN 0	P0_VID_IN_A	P0_VID_IN_B	Video input A or B for path 0 (AC or DC) (monochrome or red input).
VID IN 1	P1_VID_IN_A	P1_VID_IN_B	Video input A or B for path 1 (AC or DC) (monochrome or green input).
TRIG 0/2	P0_TTL_AUX(TRIG)_IN	P2_TTL_AUX(TRIG)_IN	TTL trigger input for PSG 0 or 2.
EXP 0/2	P0_TTL_AUX(EXP)_OUT	P2_TTL_AUX(EXP)_OUT	TTL exposure output for PSG 0 or 2.
VID IN 2	P2_VID_IN_A	P2_VID_IN_B	Video input A or B for path 2 (AC or DC) (monochrome or blue input).
VID IN 3	P3_VID_IN_A	P3_VID_IN_B	Video input A or B for path 3 (AC or DC) (monochrome input).
TRIG 1/3	P1_TTL_AUX(TRIG)_IN	P3_TTL_AUX(TRIG)_IN	TTL trigger input for PSG 1 or 3.
EXP 1/3	P1_TTL_AUX(EXP)_OUT	P3_TTL_AUX(EXP)_OUT	TTL exposure output for PSG 1 or 3.

Important

To connect the output of a display board (with a DVI output connector) to the analog video input connectors, you can use a standard cable (DVI-I to DVI-I or DVI-A to DVI-A cable) if the display board encodes the synchronization signals on the video data (sync on green). Otherwise, you must use the Matrox DVI-TO-8BNC/O cable or a custom cable that re-routes the synchronization signals to the appropriate pins.

Connecting to Matrox Helios XD

The Matrox Helios XD board has the following connectors:

- **Digital video input connector 0 (100-pin).** Used to receive video input (for acquisition paths 0 and 1), timing, and synchronization signals and transmit/receive communication signals between the video source and the frame grabber.

- **Internal digital video input connector (100-pin on the top edge).** Used to receive video input (for acquisition paths 2 and 3), timing, and synchronization signals and transmit/receive communication signals between the video source and the frame grabber. The connector is located on the edge of the board, making the signals accessible from inside the computer enclosure.

- **Internal auxiliary I/O connector (50-pin on the top edge).** Used to transmit timing and synchronization signals, and transmit/receive auxiliary signals. The connector is located on the edge of the board, making the signals accessible from inside the computer enclosure.

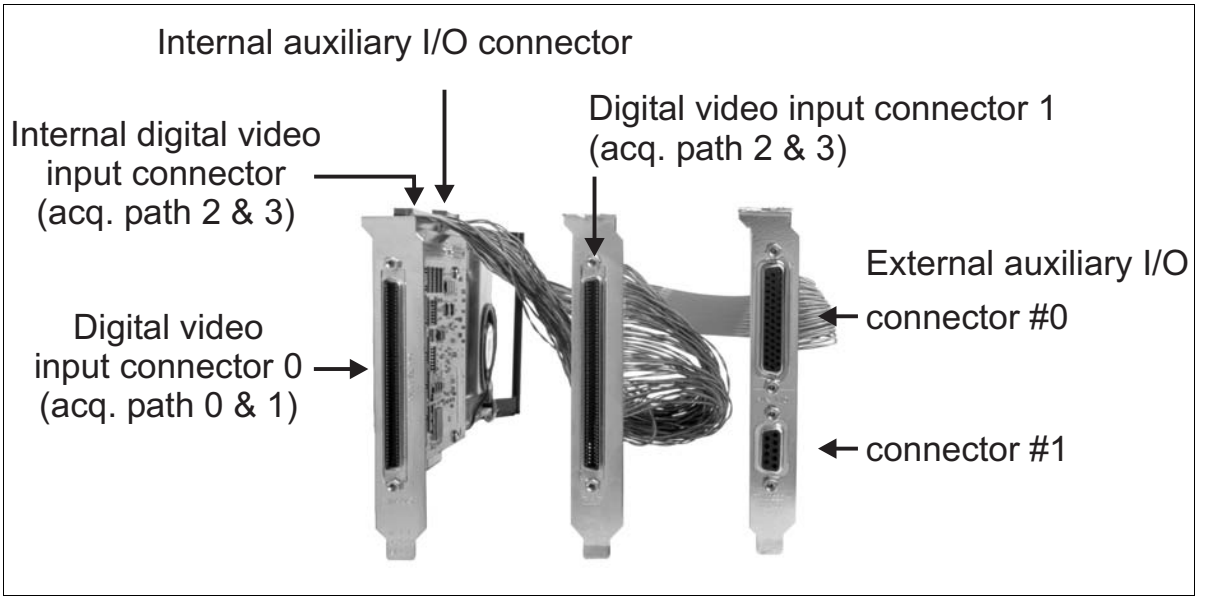
- **System reset connector.** Used to reset the motherboard if the reset button is pressed or the Watchdog circuitry of Matrox Helios detects abnormal Host inactivity.

To access the signals of the internal digital video input connector from outside of the computer enclosure, you might have installed the digital video input adapter board. It has the following connector:

- **Digital video input connector 1 (100-pin).** Used to receive video input (for acquisition paths 2 and 3), timing, and synchronization signals and transmit/receive communication signals between the video source and the frame grabber.

To access the signals of the internal auxiliary I/O connector from outside of the computer enclosure, you might have installed the corresponding adapter board. It has the following connectors:

- **External auxiliary I/O connector 0 (HD-44).** Used to transmit timing and synchronization signals, and transmit/receive auxiliary signals.
- **External auxiliary I/O connector 1 (DB-9).** Used to transmit/receive auxiliary signals.



You can use the Matrox DBHD100-TO-OPEN cable to connect your video sources to a digital video input connector. This cable has a 100-pin low-profile IDC connector at one end, and open-ended wires at the other end.

Chapter

3

Using multiple Matrox Helios boards

This chapter explains how to use multiple Matrox Helios boards.

Multiple board installation

You can install and use multiple Matrox Helios boards in one computer.

To use multiple Matrox Helios boards, install each additional Matrox Helios board as you installed the first board (refer to Chapter 2). Theoretically, you can have as many as 16 Matrox Helios boards installed in your computer at one time; this number is, however, limited by the number of empty slots in your computer and, for simultaneous image capture, by the available bandwidth of your PCI/PCI-X interface (segment), as discussed in the next section.

Using MIL-Lite, you have to allocate a MIL system for each board and allocate the resources of each MIL system. For more information, see *MsysAlloc()* in the MIL Reference.

Simultaneous image capture from different boards

You can simultaneously capture images from video sources attached to different Matrox Helios boards; however, the number of video sources from which you can simultaneously capture images is determined by the available bandwidth of your PCI/PCI-X segment.

Matrox Helios is susceptible to PCI/PCI-X bus latency. In addition, sustained PCI/PCI-X transfers to Host memory require the use of a high performance PCI/PCI-X core-logic chipset, such as the Intel E7500 series, ServerWorks (HE, LE, LC, or HE SL), or ServerWorks GC (HE, LE, WS, or SL). If a high performance chipset and a 133 MHz 64-bit PCI-X slot is used with a Matrox Helios board, you should not have any PCI bandwidth problems. Otherwise, it depends on the required bandwidth of the video sources used and the bandwidth of the PCI/PCI-X segment. To estimate the available bandwidth of the PCI/PCI-X segment used by your Matrox Helios board, you can use the HeliosBench tool integrated in the MIL Configuration utility.

As a reference point, capturing from a 1 Kbyte x 1 Kbyte, 8-bit, 60 frames/sec video source will require a bandwidth of 60 Mbytes/sec.

Chapter

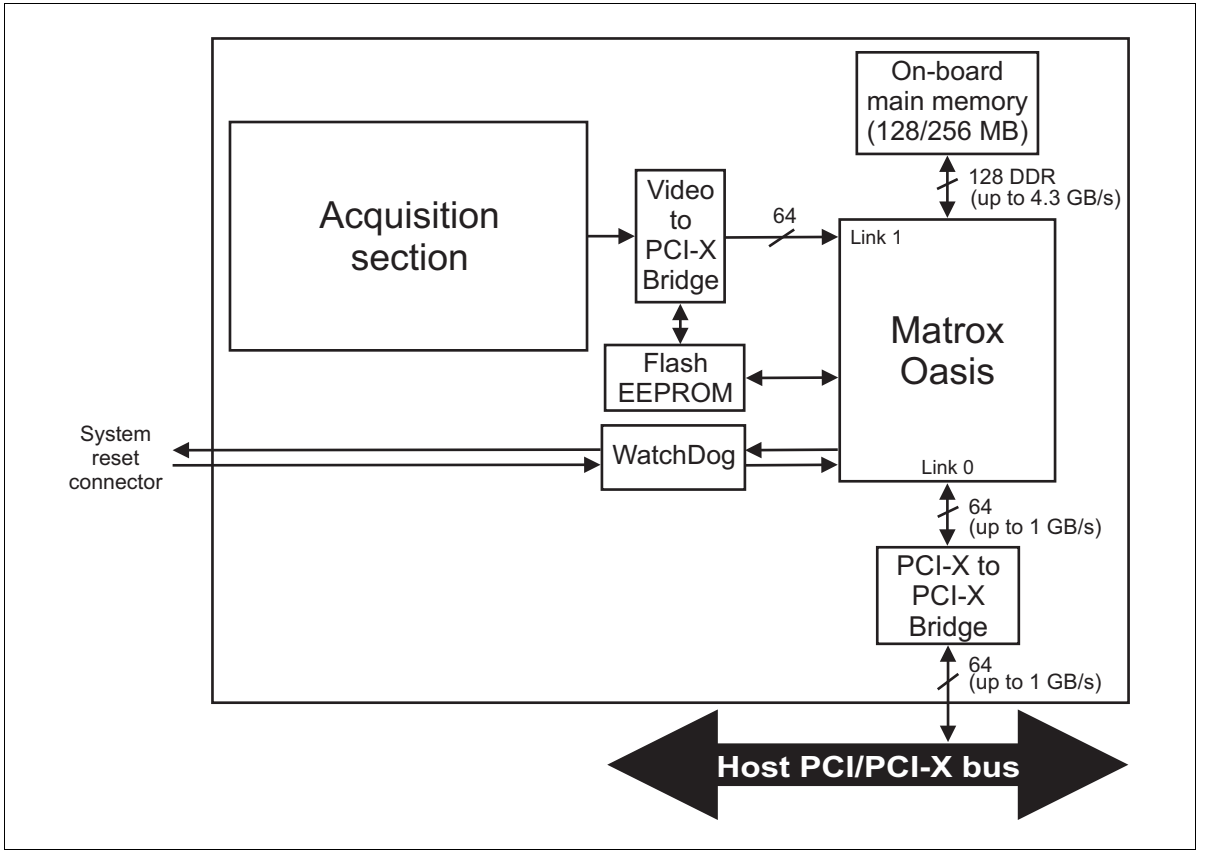
4

Matrox Helios hardware reference

This chapter explains the architecture, features and modes of the Matrox Helios XCL, XA, and XD hardware.

Matrox Helios hardware reference

This chapter provides information on the architecture of the Matrox Helios hardware. It covers the architecture, features, and modes of the acquisition section of Matrox Helios XCL, Matrox Helios XA, and Matrox Helios XD. In addition, it covers the Matrox Helios hardware related to the preprocessing and transfer of data.



A summary of the features of Matrox Helios, as well as pin assignments for the various connectors, can be found in Appendix B.

Acquisition path

This manual uses the term acquisition path to refer to a path that has the components to, for example, digitize or capture a video input signal. The term *independent acquisition path* is used to refer to an acquisition path that can, if required, acquire data from an input source independently from another such path on the same frame grabber. Each independent acquisition path has its own programmable synchronization generator (PSG) to manage all video timing, synchronization, triggering, exposure, and user-defined input and output signals for the path.

MIL-Lite uses the concept of a MIL digitizer to represent the acquisition path(s) with which to grab from one input source of the specified type. When several MIL digitizers are allocated, their device number along with their DCF identify if they represent the same path(s) (but perhaps for a different input format) or independent path(s) for simultaneous acquisition. MIL-Lite uses the concept of a data input channel to identify which input source to use when several of its type can be connected to the same acquisition path(s) (for example, grab from channel 0 or channel 1 of digitizer 0).

Digitizer configuration format

To program the acquisition section, allocate a MIL digitizer using **MdigAlloc**() with an appropriate DCF (supplied or created) and digitizer device number; to select the required input channel, use **MdigChannel**(). If you find a DCF file that is suitable for your video source, but you need to adjust some of the more common settings, you can do so directly, without adjusting the file, using the appropriate MIL-Lite function. For more specialized adjustments, use the Matrox Intellicam program to adjust the DCF file. Using Matrox Intellicam, you can set the active video region, the sampling clock, and all the other parameters related to the timing of the video signal (that is, standard and non-standard video, interlaced or non-interlaced) in your DCF file.

Matrox Helios XCL acquisition section

Matrox Helios XCL can capture video from digital video sources compliant with the Camera Link Specification. Matrox Helios XCL supports monochrome and component RGB acquisition. Besides standard Camera Link video sources, it also supports additional types of video sources, including time-multiplexed video sources.

Matrox Helios XCL is available in two versions: a dual-Base version and a single-Full version. The dual-Base version has two independent Camera Link acquisition paths that feature two Base configurations. The single-Full version has one acquisition path that supports all configurations: Base, Medium, and Full. Unless otherwise specified, the following discussion applies to both versions of Matrox Helios XCL.

Each acquisition path can grab at a maximum rate of 85 Mega-samples/sec. Each acquisition path has its own programmable synchronization generator (PSG), formatters, and LUTs, and can have a different acquisition rate. Matrox Helios XCL supports a comprehensive set of general purpose I/O and serial ports to control cameras and other video sources.

Performance

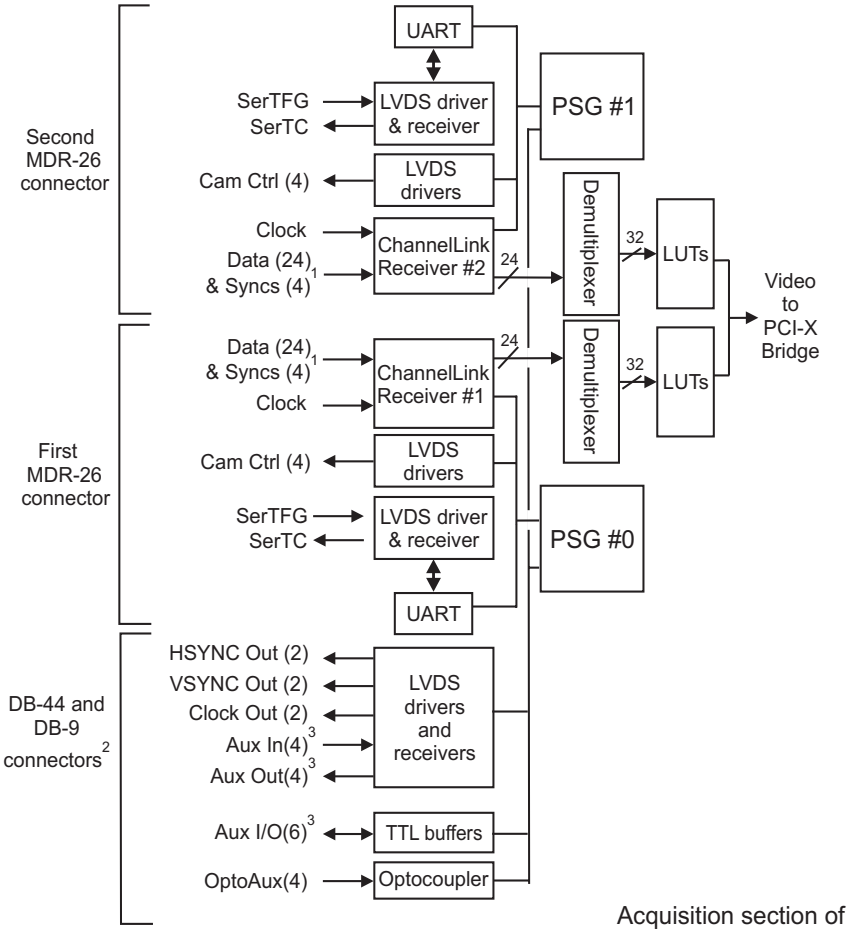
The video timing parameters supported by the board are as follows:

	Maximum
Number of pixels / line (including sync and blanking)	16 M
Number of lines / frame (including sync and blanking)	1 M
Pixel clock	85 MHz
Bandwidth for single-Full version	680 Mbytes/sec
Bandwidth for dual-Base version	510 Mbytes/sec

Dual-Base version

The dual-Base version supports simultaneous acquisition from two video sources, for a maximum of 24 bits of video data from each. When acquiring from time-multiplexed video sources, a maximum of 32 bits of video data is supported

from each. The video sources can be frame, field, or line-scan video sources. Note that the acquisition paths are completely independent, and therefore the video sources do not need to be identical.

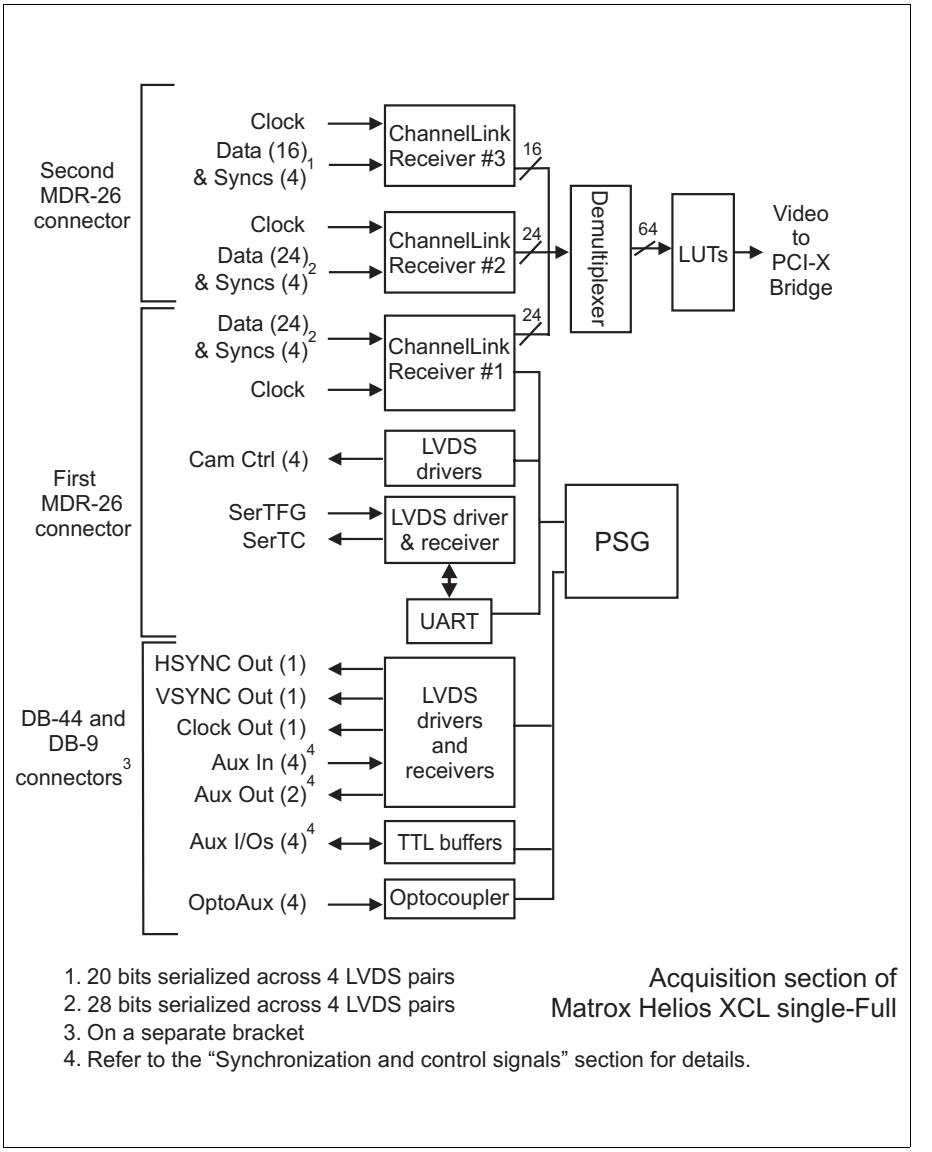


Acquisition section of Matrox Helios XCL dual-Base

1. 28 bits serialized across 4 LVDS pairs
2. On a separate bracket
3. Refer to the “Synchronization and control signals” section for details.

Single-Full version

The single-Full version allows you to grab from one video source, up to 64 bits of video data. The video source can be a frame, field, or line-scan video source. Note that in the Medium and Full configuration, one video source uses the two Camera Link connectors.



1. 20 bits serialized across 4 LVDS pairs
2. 28 bits serialized across 4 LVDS pairs
3. On a separate bracket
4. Refer to the “Synchronization and control signals” section for details.

Acquisition section of Matrox Helios XCL single-Full

Video sources supported by the dual-Base version

The dual-Base version accepts the following video sources for each acquisition path:

	Video sources supported per acquisition path
Camera Link Standard	• One tap x 8/10/12/14/16-bit. • Two tap x 8/10/12-bit. • One 3 x 8-bit (RGB).
Not Camera Link Standard	• Two tap 14/16-bit with time-multiplexing. • Four tap 8-bit with time-multiplexing.

Video sources supported by the single-Full version

In addition to the video sources supported by the dual-Base version, the single-Full version supports the following video sources:

	Video sources supported
Camera Link Standard	• Eight tap x 8-bit. • Four tap x 8/10/12-bit. • One 3 x 10/12-bit (RGB).
Not Camera Link Standard	• 8 tap x 8-bit with time-multiplexing (using only 2 receivers). • Four tap 10/12-bit with time-multiplexing. • Two tap x 14/16-bit. • One 3 x 14/16-bit (RGB). • Two 3 x 8-bit (RGB) (genlocked).

ChannelLink receivers

The dual-Base version of the board uses two standard ChannelLink receivers for video input(s), while the single-Full version uses three. The dual-Base version can operate the two receivers asynchronously, whereas single-Full version operates them synchronously.

Each receiver can receive up to 24 bits of video data and 4 bits of synchronization and field data, as serialized data over four LVDS pairs from the video source. A clock is received from the video source over a fifth LVDS pair.

Demultiplexers

Each acquisition path of the board features a demultiplexer. It can deserialize input from time-multiplexed video sources on a clock basis; time-multiplexed video sources can output twice the amount of data as other video sources with less cabling. When enabled, the demultiplexer assumes that two video streams share the same data path and that the streams are interleaved based on the clock cycle. The demultiplexer assumes that on one clock cycle, the data is from one stream and that on the next clock cycle, the data is from the second stream. The demultiplexer combines the data from the two streams every second clock cycle and sends them to the LUTs. The demultiplexer can only deserialize video inputs that when combined, total a maximum depth of 32 bits per acquisition path on the dual-Base version or a maximum depth of 64 bits on the single-Full version.

Lookup tables

The board has four 256-entry 8-bit programmable lookup tables (LUTs) and four 4096 entry 8- or 16-bit LUTs.

On the dual-Base version, the LUTs can be operated in the following configurations per acquisition path:

- 8 palettes of one, two, three, or four 256-entry 8-bit LUTs.
- 4 palettes of one or two 1024 entry 8- or 16-bit LUTs.
- 1 palette of one or two 4096 entry 8- or 16-bit LUTs.

On the single-Full version, the LUTs can be operated in the following configurations:

- 8 palettes of one, two, three, four, or eight 256-entry 8-bit LUTs.
- 4 palettes of one, two, three, or four 1024-entry 8- or 16-bit LUTs.
- 1 palettes of one, two, three, or four 4096 entry 8- or 16-bit LUTs.

14- and 16-bit data by-pass the LUTs.

The LUTs are programmed using the MIL-Lite function **MdigLut**().

Communication

For each acquisition path, two LVDS pairs are used to transmit or receive asynchronous serial communication between the video source and the board. These signals are handled by the Universal Asynchronous Receiver/Transmitter(s) (UARTs).

For each acquisition path, four camera control output signals are also available. These are general-purpose signals that are sent to the video source.

UARTs

The dual-Base version of Matrox Helios XCL offers two LVDS compatible serial interfaces, whereas the single-Full version features only one. Each interface is mapped as a COM port so that it can be accessed through the Win32 API. Each interface is comprised of both a transmit port and a receive port, permitting the interface to work in full-duplex mode.

Each interface is controlled by a Universal Asynchronous Receiver-Transmitter (UART). Each UART features independently programmable baud rates; each supports all standard baud rates from 300 baud up to 115200[1] baud. Each has an internal 8-byte FIFO memory buffer. In addition, each can generate system level interrupts in both transmit and receive operations.

PSGs

The dual-Base version of Matrox Helios XCL features two Programmable Synchronization Generators (PSGs), whereas the single-Full version features only one PSG. The PSGs are responsible for managing all video timing, synchronization, triggering, exposure, and user-defined input and output signals.

Each PSG allows for independent acquisition from video sources. Therefore, the dual-Base version allows acquisition from two independent video sources, whereas the single-Full version allows acquisition from only one video source.

1. Note that the maximum baud rate is highly dependant on the amount of computer resources available.

Synchronization and control signals

The following tables summarize the synchronization, timing, and control signals supported by Matrox Helios XCL. Most of these signals are available by defining camera control or auxiliary (general purpose) signals as such in the DCF. When an acquisition path supports several signals of a specific type, the tables identify the one to which an auxiliary/camera control signal can be defined. For example, for acquisition path 0, you can define P0_TTL_AUX_IO_1 as exposure output 0 and TTL_AUX_IO_0 as exposure output 1. Note, signals defined for acquisition path 1 do not apply to the single-Full version. *CL connect.* stands for Camera Link connector.

			LVDS cam. ctrl								TTL aux. I/O[2]						OPTO aux. in[2]				LVDS aux. in[2]				LVDS aux. out[2]			
			CL connect. 0				CL connect. 1																					
Type of signal	**Path#**	**Max # signals[1]**	**CC1**	**CC2**	**CC3**	**CC4**	**CC1**	**CC2**	**CC3**	**CC4**	**P0_TTL_AUX_IO_0[3]**	**P0_TTL_AUX_IO_1**	**P1_TTL_AUX_IO_0**	**P1_TTL_AUX_IO_1**	**TTL_AUX_IO_0**	**TTL_AUX_IO_1**	**P0_OPTO_AUX_IN0[3]**	**P0_OPTO_AUX_IN1[3]**	**OPTO_AUX_IN0**	**OPTO_AUX_IN1**	**P0_LVDS_AUX_IN0[3]**	**P0_LVDS_AUX_IN1**	**LVDS_AUX_IN0**	**LVDS_AUX_IN1**	**P0_LVDS_AUX_OUT0**	**P0_LVDS_AUX_OUT1**	**P1_LVDS_AUX_OUT0**	**P1_LVDS_AUX_OUT1**
Exposure output	0	2	0/1	0/1	0/1	0/1						0			1										0	1		
	1	2					0/1	0/1	0/1	0/1				0		1											0	1
Trigger input	0	4									0	1			2	3	0	1	2	3	0	1	2	3				
	1	4											0	1	2	3			0/2	1/3			0/2	1/3				
Field polarity input	0	1									0						0				0							
	1	1											0						0				0					
Timer clock input	0	1																				0						
	1	1																						0				
Quadrature input[4]	0	1																			0	1						
	1	1																					0	1				
User input	0	12									2	3			4	7	0	1	8	9	5	6	10	11				
	1	8											2	3	7	4			0	1			5	6				
User output	0	7	0/1	0/1	0/1	0/1					2	3			4	7									5	6		
	1	7					0/1	0/1	0/1	0/1			2	3	7	4											5	6

1. The maximum # for each signal type cannot always be attained. The actual maximum depends on whether the required auxiliary signals are available or have been defined as another type.
2. On external auxiliary I/O connector 0 (DB-44).
3. On external auxiliary I/O connector 1 (DB-9).
4. Note that a rotary encoder with quadrature output transmits a two-bit code so table entries denoted bit position.

Type of signal	Path#	Max # signals[1]	LVDS cam. ctrl								Received with data		LVDS dedicated signals[2 3]
			CL connect. 0				CL connect. 1						
			CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4	CL connect. 0	CL connect. 1	
Frame valid input	0	1									0		
	1	1										0	
VSYNC output	0	1	0	0	0	0							P0_LVDS_VSYNC_OUT
	1	1					0	0	0	0			P1_LVDS_VSYNC_OUT
Line valid input	0	1									0		
	1	1										0	
HSYNC output	0	1	0	0	0	0							P0_LVDS_HSYNC_OUT
	1	1					0	0	0	0			P1_LVDS_HSYNC_OUT
Data valid input	0	1									0		
	1	1										0	
Clock input	0	1											Xclk (CL connect. 0) and Yclk[4] and Zclk[4] (CL connect. 1)
	1	1											Xclk (CL connect. 1)
Clock output	0	1	0	0	0	0							P0_LVDS_CLK_OUT
	1	1					0	0	0	0			P1_LVDS_CLK_OUT

1. The maximum # for each signal type cannot always be attained. The actual maximum depends on whether the required auxiliary signals are available or have been defined as another type.
2. In this column, each signal is a dedicated signal (that is, it cannot be redefined as another type of signal).
3. Clock input is received on the Camera Link connectors, whereas the other signals in this column are received on/transmitted from external auxiliary I/O connector 0 (DB-44).
4. For the single-Full version only.

Camera control

As mentioned previously, for each acquisition path, the board supports four camera control output signals. You can route exposure signals, synchronization output signals, or user-defined signals to these signals. You specify their purpose in the DCF file. You can then program them using the MIL-Lite function **MdigControl**() with M_USER_... or M_GRAB_EXPOSURE....

Auxiliary input and output signals

In addition, the board supports auxiliary multi-purpose input and output signals. Auxiliary output signals can be routed as exposure signals or user-defined signals (for controlling external devices, such as a strobe light or programmable logic controller). Auxiliary input signals can be routed as trigger input (for example, to

synchronize image acquisition with external events), quadrature input, field polarity, timer clock input, or user-defined signals (for example, to synchronize an application with a user-defined event).

The board supports auxiliary signals in different formats:

Auxiliary signals	# per path	# total
LVDS camera control signals (output).	4	8
TTL auxiliary input or output signals.	2 (+2 depending on type of signal)	6
Opto-isolated auxiliary input signals.	depends on type (2 reserved for P0, 2 not specified)	4
LVDS auxiliary input signals.	depends on type (2 reserved for P0, 2 not specified)	4
LVDS auxiliary output signals.	2	4

Note that the opto-isolated signals pass through an opto-coupler, a device that protects the board from outside surges and different ground levels, and permits total electrical isolation from the frame grabber.

You specify the purpose of the auxiliary signals in the DCF. You can then program these signals using the MIL-Lite function **MdigControl**() with M_USER..., M_TRIGGER..., or M_GRAB_EXPOSURE....

Trigger

For each PSG, you can program two auxiliary signals as external trigger inputs. For each PSG, you can also program two path-independent auxiliary signals as trigger inputs.

Each PSG can operate in one of the two following trigger modes; the mode is specified by the DCF:

- **Next valid frame/field mode.** In this mode, the board waits for the next valid frame or field (as specified by the DCF file) before commencing the grab. This trigger mode functions in one of three ways:

  - **Edge-triggered monoshot acquisition.** The board waits for the rising/falling edge to capture a single frame.

  - **Edge-triggered continuous acquisition.** The board waits for the rising/falling edge to start a continous grab.

  - **Level-sensitive continuous acquisition.** The board grabs continuously while the level of the trigger is high/low.

  ❖ The polarity of the active and inactive levels of the trigger signal is software programmable.

- **Asynchronous reset mode.** In this mode, the board resets the video source to begin a new frame when the trigger signal is received.

Trigger format

When received in TTL format directly, the signal must have a maximum amplitude of 5 V. A signal over 2 V is considered high, while anything less than 0.8 V is considered low; the transition of 0.8 V to 2 V is considered to be the rising edge.

If using the trigger to start acquisition, the trigger signal's pulse width must be greater than two pixels; if using the trigger to start the exposure timer, the trigger signal's pulse width must be greater than two clock periods of the timer. To determine the timer period, take the inverse of the pixel or timer's clock frequency, respectively. For example, if the pixel frequency is 12.27 MHz, the minimum pulse width is 2 x 1/12.27 MHz (approximately 164 nsec).

The opto-isolated trigger signals pass through an opto-coupler. The voltage difference across the positive and negative components of the signal must be between 4.06 V and 9.165 V for logic high, and between -5.0 V and 0.8 V for logic low.

Exposure

Each PSG has two exposure timers. These timers can each generate two periodic exposure output signals to control the exposure time and other external events related to the video source. The exposure signals can be output as control signals on the video input Camera Link connectors; they can also be output using auxiliary output signals.

The timers can use a clock that is internally generated or one from an external source. In the latter case, you can define an auxiliary signal as the clock source (timer clock input).

Synchronization

For each PSG, the board can supply one horizontal (HSYNC) and one vertical (VSYNC) synchronization signal to the video source. Through the Camera Link connectors, the board also receives synchronization data (frame valid, line valid, and data valid) along with the video data; refer to the Camera Link specification for a description of the synchronization data.

Note that the Camera Link standard does not regulate how to transmit an interlaced video signal, however you can define an auxiliary signal as a field polarity input signal and transmit the field polarity on this signal.

Clock

For each PSG, the board can supply a clock signal to the video sources. Through each of the video input Camera Link connectors, the board can also receive a clock signal.

Quadrature decoder

Each PSG features a quadrature decoder that can decode input from a rotary encoder with quadrature output. A rotary encoder (sometimes called a quadrature encoder) is a device that provides information about the position of a rotating shaft. The encoder outputs a two-bit code (also known as gray code) on two pairs of LVDS wires in a precise sequence: 00 01 11 10. The sequence determines the position of the rotating shaft and the direction of rotation.

The quadrature decoder can decode gray code and update a 16-bit internal counter. You can read the counter at different stages of the grab or trigger a grab based on the value of the counter. The quadrature decoder can support a maximum encoder frequency equal to the pixel clock frequency for the camera.

- You cannot power the rotary encoder using the Matrox Odyssey grab module; an external source must be used (for example, the computer's 5 V power source).

For each PSG, you can program two auxiliary signals as quadrature inputs. One to carry the first bit, and one to carry the second. Quadrature decoder settings can be toggled using **MdigControl**(), or by modifying the DCF file.

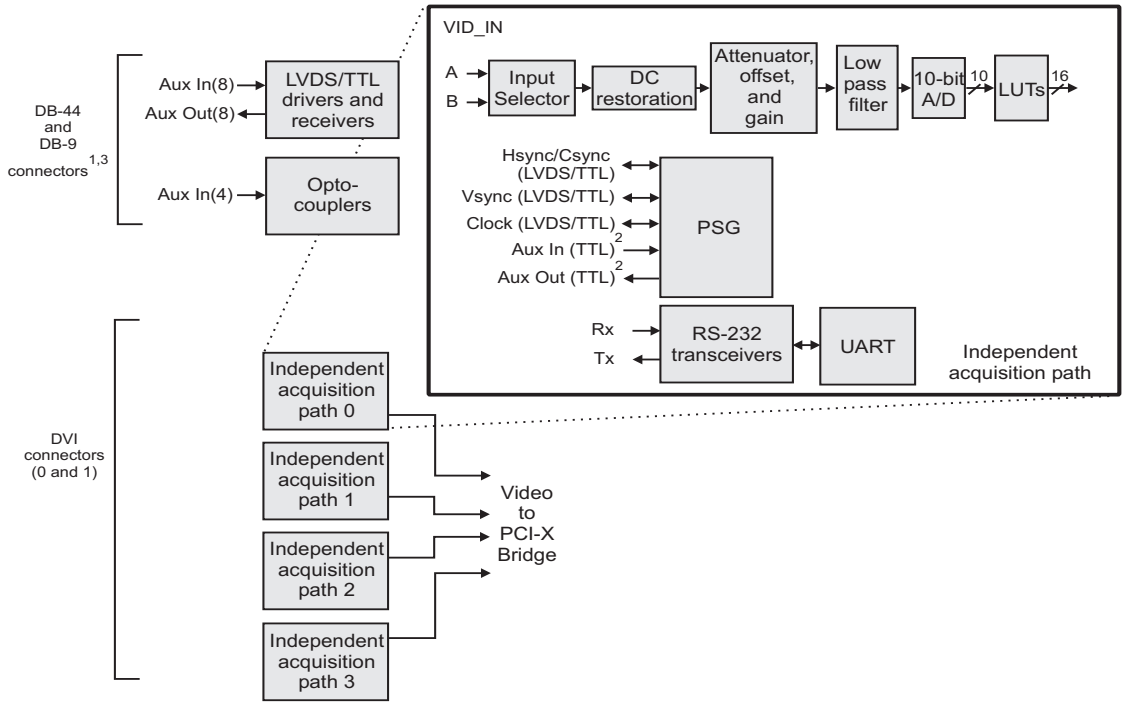
Matrox Helios XA acquisition section

Matrox Helios XA has four completely independent acquisition paths, allowing simultaneous acquisition from four independent video sources. The video sources can be standard or non-standard video sources.

Each acquisition path has two selectable inputs (A or B), and performs AC or DC coupling on each one. In addition, each acquisition path digitizes at a 10-bit pixel resolution; the most-significant 8 bits or all 10 bits can be stored. Each acquisition path has its own filters, programmable gain, and LUTs.

Matrox Helios XA supports video sources with up to 4 taps, and can grab at a maximum rate of 80 Mega-samples/sec. By driving the same video signal to A/Ds that are using two phase-shifted timing sources, you can double the nominal acquisition rate.

In addition, Matrox Helios XA has a comprehensive set of general purpose I/O and serial ports to control video sources and other devices.



1. On a separate bracket.
2. Refer to the “Synchronization and control signals” section for details.
3. Dependency on acquisition path is not illustrated.
   Refer to the “Synchronization and control signals” section.

Acquisition section of Matrox Helios XA

Performance

The video timing parameters supported by the board are as follows:

	Maximum
Number of pixels / line (including sync and blanking)	2 M
Number of lines / frame (including sync and blanking)	1 M
Pixel clock for single sampling rate operation	80 MHz
Pixel clock for double sampling rate operation	160 MHz
Analog bandwidth (-3 db cutoff frequency)	140 MHz

Analog input

Matrox Helios XA includes the electronic circuitry needed to select, amplify, filter, and drive the video signal prior to sending it to the analog-to-digital (A/D) converters.

Matrox Helios XA has four wide-band (140 MHz) analog acquisition paths. The following tables describe the video source combinations from which simultaneous, independent aquisition is supported and the acquisition paths to which they must be connected:

Configuration	Asynchronous video sources supported [1]	Acquisition path			
		0	1	2	3
1	1 4-tap video source	4-tap			
2	1 3-tap video source (RGB) and 1 1-tap video source	3-tap			1-tap
3	2 2-tap video sources	2-tap		2-tap	
4	1 2-tap video source and 2 1-tap video sources	2-tap		1-tap	1-tap
5	1 2-tap video source and 2 1-tap video sources	1-tap	1-tap	2-tap	
6	4 1-tap video sources	1-tap	1-tap	1-tap	1-tap

1. Note that taps expected to come from the same video source can also come from different video sources as long as they are synchronized (genlocked). In this case, the grabbed data is stored in separate color bands of the same buffer; the buffer can be in planar format.

The analog input section can also be configured so that the same video signal drives two analog-to-digital converters (A/Ds). By using two A/Ds to sample the same video signal and clocking each A/D with a different phase-shifted clock, the overall effective sampling rate can be doubled.

Sampling rate	# of acquisition paths available	Acquisition path #	# of A/Ds per acquisition paths used
80 MHz	4	0, 1, 2, 3	1
160 MHz	2	0 or 2	2

The pixel clock setting automatically determines how many A/Ds are used per acquisition path. For example, by specifiying a pixel clock in the range of 81 MHz to 160 MHz, two A/D's are automatically selected. The pixel clock setting is specified in the DCF.

Input voltage level and protection

The various amplification stages on Matrox Helios XA are able to provide a maximum peak signal of 3V without saturation. Any positive video signal level greater than this threshold will be distorted, so it is not recommended to feed a signal above 3V with termination (6 V unterminated).

Clamping diodes protect video inputs from overvoltage. The diodes clamp (clip) the inputs if they go under -5 V or above +5 V. When there is overvoltage, the maximum current flowing must be no more than 0.5A, otherwise damage can occur to the board.

Selectable inputs

Each acquisition path can acquire data from one of two possible input sources (A or B); each is 75-Ohm terminated. The signal coupling of each input can be either capacitor coupled (AC coupling) or directly coupled (DC coupling), single ended. A multiplexer allows the input source selection and the AC/DC coupling selection.

AC coupling transmits the varying (AC) characteristics of the signal while blocking the static (DC) characteristics. This produces a signal that has an average DC level of 0 Volts regardless of average picture level or DC offset of the incoming signal. In effect, this ensures that the average surface area of the signal above 0 Volts is the same as the average surface area below 0 Volts.

AC coupling is implemented using a series capacitor. The capacitor is a first order high-pass filter with a 0.8 Hz -3dB cutoff frequency. The high-pass frequency cutoff is 0.8 Hz to allow all frequency components of a frame with a 3 kHz line rate to pass with less than 0.3% attenuation.

DC restoration

After the signal undergoes AC coupling or DC coupling, the signal can be DC restored. While AC-coupled signals require DC restoration to retrieve the DC level of the original video signal, DC restoration can be useful for DC-coupled signals to compensate for any DC offset (although not required). You can enable or disable DC restoration independently of the input coupling selection.

To perform DC restoration, the board samples the signal during each scanned line in the specified region, and vertically shifts the signal so that this region is at either 0 or 1 V, depending on which of the two restoration levels has been specified. If the synchronization pulse is negative with non-inverted video, you should set the

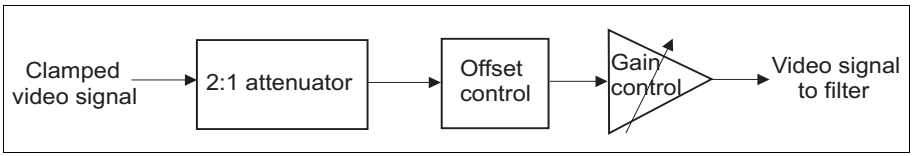
DC restoration level to 0 V to have positive active video. If the synchronization pulse is positive with a negative video signal, set the restoration level to 1 V so that most of the video signal is above 0 V.

Note that DC restoration requires a reference region in the video signal, usually the black portion of a frame. When using a non-standard signal source, such a reference region might not be present. For these special cases, you should disable DC restoration.

You specify whether DC restoration should be enabled, the DC restoration level, and the reference region in the DCF file.

Adjusting the reference levels

For each acquisition path, you can adjust the signal's black and white reference levels so that the full dynamic range of each 10-bit A/D is used. Matrox Helios XA uses the offset-gain topology to adjust the black and white reference levels of the signal. The topology uses a variable offset controller followed by a variable gain controller; the signal can be routed through an optional 2:1 attenuator prior to being offset.



The variable offset controller vertically shifts the entire signal so that you can set the lowest part of the video signal to 0 V, which is at the bottom of the A/D conversion range. The offset adjustment range is -1 V to +1 V, in 4096 steps (12-bit resolution).

The variable gain controller can then amplify the signal so that you can set the highest part of the video signal to 1 V, which is at the top of the A/D conversion range. The gain adjustment range is between 0 and 4, in 4096 step increment (12-bit resolution).

Before passing to the offset block, the signal can be routed through an attenuator. The attenuator is a 2:1 voltage divider. The attenuator is present because the variable gain controller cannot accept a positive or negative signal with an amplitude above 1.2 V without distortion. The attenuator allows you to pass a

signal up to 2.4 V in amplitude (active video) without distortion. If the active input video (excluding the sync pulse) is greater than 1.2 V in amplitude, the attenuator should be enabled.

The maximum gain factors and the recommended video signal amplitude are as follows:

2:1 attenuator	Maximum gain	Max recommended video signal amplitude (terminated)	Min recommended video signal amplitude
Off (bypassed)	4	1.2 V	0.25 V
On (active)	2	2.4 V	0.5 V

There are three ways to program the reference levels and the attenuator. You can specify the actual black and white voltage levels of your input signal and have the software calculate appropriate values for each element in the offset-gain topology. You can have the software emulate an A/D with programmable black and white references and specify the levels as a percentage of their possible values. Alternatively, you can specify the required values for the offset and the gain controls. If the signal amplitude is specified as greater than 1.1 V, the attenuator will be enabled automatically. In all cases, you use the MIL-Lite function **MdigReference**() or **MdigControl**().

Low-pass filter

The low-pass filtering stage is used to limit high frequency noise and aliasing effects at the input of the A/D converter. Each acquisition path has two filters. The filters used on Matrox Helios are 4th order Butterworth filters. The first has a -3 dB cutoff frequency of 40 MHz. The second filter has a -3 dB cutoff frequency of 7.5 MHz, useful for RS-170 and CCIR video sources. All filters provide 80 dB/decade or 24 dB/octave of attenuation for frequencies above the cutoff value. Enable the low-pass filters using the MIL-Lite function **MdigControl**() with M_INPUT_FILTER.

10-bit A/D converters

Matrox Helios XA uses high-quality, high-speed, 10-bit analog-to-digital (A/Ds) converters to sample the video signal. Therefore, Matrox Helios XA provides excellent digitization quality, even at the highest sampling frequency. The A/D converters also feature a wideband input section, allowing full use of their sampling speed.

Lookup tables

Matrox Helios XA has four 4096 entry 8- or 16-bit programmable lookup tables (LUTs). The LUTs can be operated as 4 palettes of one, two, three, or four 1024 entry 8- or 16-bit LUTs.

The LUTs are programmed using the MIL-Lite function **MdigLut**().

UARTs

Matrox Helios XA offers four RS-232 compatible serial interfaces. Each interface is mapped as a COM port so that it can be accessed through the Win32 API. Each interface is comprised of both a transmit port and a receive port, permitting the interface to work in full-duplex mode. The interfaces are on the DVI connectors.

Each interface is controlled by a Universal Asynchronous Receiver-Transmitter (UART). Each UART features independently programmable baud rates; each supports all standard baud rates from 300 baud up to 115200[1] baud. Each has an internal 8-byte FIFO memory buffer. In addition, each can generate system level interrupts in both transmit and receive operations.

General synchronization

Matrox Helios XA can operate in either slave or master mode.

Slave mode

In slave mode, the video source provides the synchronization information to Matrox Helios XA. It can accept any one of the following:

- Synchronization signals encoded on one of the analog video signals provided to the board.
- Horizontal and/or vertical or composite synchronization signals supplied separately by the video source, in either TTL or LVDS format.

Master mode

In master mode, Matrox Helios XA generates the horizontal and/or vertical synchronization signals, and/or a pixel clock, and supplies them to the video source, allowing the video source to synchronize to the board.

1. Note that the maximum baud rate is highly dependant on the amount of computer resources available.

PSGs

Matrox Helios XA features four programmable synchronization generators (PSGs). The PSGs are responsible for managing all video timing, synchronization, trigger, exposure, and user-defined input and output signals. The PSGs on Matrox Helios XA allow the board to adapt to many video standards. Each PSG allows for independent acquisition from a video source. Therefore, Matrox Helios XA allows acquisition from four independant video sources.

The phase-locked loop

The high-performance, low-jitter phase-locked loop (PLL) uses frequency synthesis techniques to generate the clock signal in slave mode.

As a reference, the PLL uses the composite or horizontal video synchronization signal supplied by the video source (line-locked mode).

Since the signal from the video source is used as a reference, the PLL can produce a clock signal that is a multiple of it. In addition, using a programmable delay line, you can phase-shift the clock signal; this allows you to fine-tune the location at which the video signal is sampled so that you can compensate for errors when digitizing close to or at the Nyquist frequency.

	Specification
Operating frequency range	12 to 80 MHz
Jitter	4.6 nsec p-p absolute with RS-170 synchronization source
Phase adjustment	256 steps of 0.5 nsec

When the input source supplies a sampling clock that does not require adjustment, the PLL is bypassed to avoid adding jitter to the supplied clock.

Synchronization and control signals

The following tables summarize the synchronization, timing, and control signals supported by Matrox Helios XA. Most of these signals are available by defining auxiliary (general purpose) signals as such in the DCF. When an acquisition path supports several signals of a specific type, the tables identify the one to which an auxiliary signal can be defined. For example, for acquisition path 0, you can define P0_TTL/LVDS_AUX_OUT_0 as exposure output 0 and P0_TTL/LVDS_AUX_OUT_1 as exposure output 1.

Note that only the auxiliary signals of the first acquisition path used by a video source are available (for example, if grabbing RGB and monochrome, only the auxiliary signals for path 0 and path 3 are available).

You can set each TTL/LVDS signal individually to either LVDS or TTL format when accessed from the external auxiliary I/O connector 0 (DB-44) of the cable adapter board.

			TTL aux. input[2]				TTL aux. output[2]				Opto aux. input[3]				TTL/LVDS aux. input[4]								TTL/LVDS aux. output[4]							
Type of signal	**Path#**	**Max # signals[1]**	**P0_TTL_AUX(TRIG)_IN**	**P1_TTL_AUX(TRIG)_IN**	**P2_TTL_AUX(TRIG)_IN**	**P3_TTL_AUX(TRIG)_IN**	**P0_TTL_AUX(EXP)_OUT**	**P1_TTL_AUX(EXP)_OUT**	**P2_TTL_AUX(EXP)_OUT**	**P3_TTL_AUX(EXP)_OUT**	**P0_OPTO_AUX(TRIG)_IN**	**P1_OPTO_AUX(TRIG)_IN**	**P2_OPTO_AUX(TRIG)_IN**	**P3_OPTO_AUX(TRIG)_IN**	**LVDS/TTL_AUX_IN0**	**LVDS/TTL_AUX_IN1**	**LVDS/TTL_AUX_IN2**	**LVDS/TTL_AUX_IN3**	**LVDS/TTL_AUX_IN4**	**LVDS/TTL_AUX_IN5**	**LVDS/TTL_AUX_IN6**	**LVDS/TTL_AUX_IN7**	**P0_LVDS/TTL_AUX_OUT0**	**P0_LVDS/TTL_AUX_OUT1**	**P1_LVDS/TTL_AUX_OUT0**	**P1_LVDS/TTL_AUX_OUT1**	**P2_LVDS/TTL_AUX_OUT0**	**P2_LVDS/TTL_AUX_OUT1**	**P3_LVDS/TTL_AUX_OUT0**	**P3_LVDS/TTL_AUX_OUT1**
Exposure output	0	2					0																0	1						
	1	2						0																	0	1				
	2	2							0																		0	1		
	3	2								0																			0	1
Trigger input	0	4	0								1				2	3	2	3	2	3	2	3								
	1	4		0								1			2	3	2	3	2	3	2	3								
	2	4			0								1		2	3	2	3	2	3	2	3								
	3	4				0								1	2	3	2	3	2	3	2	3								
Field polarity input	0	1	0												0															
	1	1		0													0													
	2	1			0														0											
	3	1				0															0									
Data valid input	0	1													0															
	1	1															0													
	2	1																	0											
	3	1																			0									
Timer clock input	0	1														0														
	1	1																0												
	2	1																		0										
	3	1																				0								

Type of signal	Path#	Max # signals[1]	TTL aux. input[2]				TTL aux. output[2]				Opto aux. input[3]				TTL/LVDS aux. input[4]								TTL/LVDS aux. output[4]							
			P0_TTL_AUX(TRIG)_IN	P1_TTL_AUX(TRIG)_IN	P2_TTL_AUX(TRIG)_IN	P3_TTL_AUX(TRIG)_IN	P0_TTL_AUX(EXP)_OUT	P1_TTL_AUX(EXP)_OUT	P2_TTL_AUX(EXP)_OUT	P3_TTL_AUX(EXP)_OUT	P0_OPTO_AUX(TRIG)_IN	P1_OPTO_AUX(TRIG)_IN	P2_OPTO_AUX(TRIG)_IN	P3_OPTO_AUX(TRIG)_IN	LVDS/TTL_AUX_IN0	LVDS/TTL_AUX_IN1	LVDS/TTL_AUX_IN2	LVDS/TTL_AUX_IN3	LVDS/TTL_AUX_IN4	LVDS/TTL_AUX_IN5	LVDS/TTL_AUX_IN6	LVDS/TTL_AUX_IN7	P0_LVDS/TTL_AUX_OUT0	P0_LVDS/TTL_AUX_OUT1	P1_LVDS/TTL_AUX_OUT0	P1_LVDS/TTL_AUX_OUT1	P2_LVDS/TTL_AUX_OUT0	P2_LVDS/TTL_AUX_OUT1	P3_LVDS/TTL_AUX_OUT0	P3_LVDS/TTL_AUX_OUT1
Quadrature input[5]	0	1													0	1														
	1	1															0	1												
	2	1																	0	1										
	3	1																			0	1								
User input	0	10	0								1				2	3	4	5	6	7	8	9								
	1	10		0								1			4	5	2	3	6	7	8	9								
	2	10			0								1		4	5	6	7	2	3	8	9								
	3	10				0								1	4	5	6	7	8	9	2	3								
User output	0	3					2																0	1						
	1	3						2																	0	1				
	2	3							2																		0	1		
	3	3								2																			0	1

1. The maximum # for each signal type cannot always be attained. The actual maximum depends on whether the required auxiliary signals are available or have been defined as another type.
2. On analog video input connectors (DVI).
3. On external auxiliary I/O connector 1 (DB-9)
4. On external auxiliary I/O connector 0 (DB-44).
5. Note that a rotary encoder with quadrature output transmits a two-bit code so table entries denote bit position.

Type of signal	Path#	Max # signals[1]	TTL/LVDS dedicated input/ output signals[2]	TTL/LVDS aux. input[3]								TTL/LVDS aux. output[3]							
				LVDS/TTL_AUX_IN0	LVDS/TTL_AUX_IN1	LVDS/TTL_AUX_IN2	LVDS/TTL_AUX_IN3	LVDS/TTL_AUX_IN4	LVDS/TTL_AUX_IN5	LVDS/TTL_AUX_IN6	LVDS/TTL_AUX_IN7	P0_LVDS/TTL_AUX_OUT0	P0_LVDS/TTL_AUX_OUT1	P1_LVDS/TTL_AUX_OUT0	P1_LVDS/TTL_AUX_OUT1	P2_LVDS/TTL_AUX_OUT0	P2_LVDS/TTL_AUX_OUT1	P3_LVDS/TTL_AUX_OUT0	P3_LVDS/TTL_AUX_OUT1
VSYNC	0	1 in +1 out	P0_LVDS_TTL_VSYNC_IO		in								out						
	1	1 in + 1 out	P1_LVDS_TTL_VSYNC_IO				in								out				
	2	1 in + 1 out	P2_LVDS_TTL_VSYNC_IO						in								out		
	3	1 in + 1 out	P3_LVDS_TTL_VSYNC_IO								in								out
CSYNC or HSYNC[4]	0	1 in + 1 out	P0_LVDS/TTL_CHSYNC_IO	in								out							
	1	1 in + 1 out	P1_LVDS/TTL_CHSYNC_IO			in								out					
	2	1 in + 1 out	P2_LVDS/TTL_CHSYNC_IO					in								out			
	3	1 in + 1 out	P3_LVDS/TTL_CHSYNC_IO							in								out	
Clock	0	1 in/out	P0_LVDS/TTL_CLK_IO																
	1	1 in/out	P1_LVDS/TTL_CLK_IO																
	2	1 in/out	P2_LVDS/TTL_CLK_IO																
	3	1 in/out	P3_LVDS/TTL_CLK_IO																

1. The maximum # for each signal type cannot always be attained. The actual maximum depends on whether the required auxiliary signals are available or have been defined as another type.
2. In this column, each signal is a dedicated signal (that is, it cannot be redefined as another type of signal). These signals can be accessed from the DVI connectors; the clock signal can also be accessed from the internal auxiliary I/O connector.
3. On external auxiliary I/O connector 0 (DB-44).
4. The board can accept an HSYNC or CSYNC input signal, but it can only output an HSYNC signal.

Auxiliary signals

The board supports auxiliary multi-purpose input and output signals. Auxiliary output signals can be routed as exposure signals or user-defined signals (for controlling external devices, such as a strobe light or PLC). Auxiliary input signals can be routed as trigger input (for example, to synchronize image acquisition with external events), quadrature input, field polarity, data valid, timer clock input, or user-defined signals (for example, to synchronize an application with a user-defined event).

The board supports auxiliary signals in different formats:

Auxiliary signals	# per path	# total
Auxiliary input signals that can be defined as either TTL or LVDS.	depends on type of signal	8
Opto-isolated auxiliary input signals.	1	4
TTL auxiliary input signals.	1	4
Auxiliary output signals that can be defined as either TTL or LVDS.	2	8
TTL auxiliary output signals.	1	4

Note that the opto-isolated signals pass through an opto-coupler, a device that protects the board from outside surges and different ground levels, and permits total electrical isolation from the frame grabber.

You specify the purpose of the auxiliary signals in the DCF. You can then program these signals using the MIL-Lite function **MdigControl**() with **M_USER...**, **M_TRIGGER...**, or **M_GRAB_EXPOSURE...**

Synchronization

Each PSG can accept and/or provide one horizontal (HSYNC) and one vertical (VSYNC) synchronization signal (slave or master mode). Instead of accepting a horizontal synchronization signal, each PSG can alternatively accept a composite (CSYNC) synchronization signal. Note also that, if the synchronization signals are encoded on the video signal, the horizontal and vertical sychronization signals are present as a composite synchronization pulse along with the video signal.

With interlaced video sources, you can typically establish which field is being input by noting the phase shift between the horizontal and the vertical synchronization signals. Alternatively, you can define an auxiliary signal as a field polarity input signal and transmit the field polarity on this signal.

To establish which pixels are active in a line (because the horizontal synchronization signal does not identify the blanking portion of the signal), the board can generate a data valid signal based on information specified in the DCF. Alternatively, you can define an auxiliary input signal as a data valid signal.

Clock

Each PSG can accept or provide one pixel clock signal (slave or master mode).

Important

When accessed from the analog video input connectors (DVI), the pixel clock, composite/horizontal synchronization, and vertical synchronization signals of each PSG form a group of signals. The signals of each group shares the same

direction (input or output) and same signal format (TTL or LVDS). When accessed from the internal or external auxiliary I/O connectors (HD-44), the format and direction of the synchronization signals are independent; the board can both transmit and receive synchronization signals at the same time.

Trigger signals

Each PSG accepts two external trigger inputs: one TTL or LVTTL trigger input and another trigger input that passes through an opto-coupler, a device that protects the board from outside surges. For each PSG, you can also program two path-independent auxiliary signals as trigger inputs; these can be received in LVDS, TTL, or LVTTL.

Each PSG can operate in one of the two following trigger modes; the mode is specified by the DCF:

- **Next valid frame/field mode.** In this mode, the board waits for the next valid frame or field (as specified by the DCF file) before commencing the grab. This trigger mode functions in one of three ways:
  - **Edge-triggered monoshot acquisition.** The board waits for the rising/falling edge to capture a single frame.
  - **Edge-triggered continuous acquisition.** The board waits for the rising/falling edge to start a continous grab.
  - **Level-sensitive continuous acquisition.** The board grabs continuously while the level of the trigger is high/low.
  - ❖ The polarity of the active and inactive levels of the trigger signal is software programmable.
- **Asynchronous reset mode.** In this mode, the board resets the video source to begin a new frame when the trigger signal is received.

Trigger format

When received in TTL format directly, the signal must have a maximum amplitude of 5 V; when received in LVTTL format directly, the signal must have a maximum amplitude of 3.3 V. A signal over 2 V is considered high, while anything less than 0.8 V is considered low; the transition of 0.8 V to 2 V is considered to be the rising edge.

If using the trigger to start acquisition, the trigger signal's pulse width must be greater than two pixels; if using the trigger to start the exposure timer, the trigger signal's pulse width must be greater than two clock periods of the timer. To determine the timer period, take the inverse of the pixel or timer's clock frequency, respectively. For example, if the pixel frequency is 12.27 MHz, the minimum pulse width is 2 x 1/12.27 MHz (approximately 164 nsec).

A trigger signal connected to external I/O connector 1 of the adapter board, passes through an opto-coupler. The voltage difference across the positive and negative components of the signal must be between 3.15 V and 6.45 V for logic high, and between -5.0 V and 0.8 V for logic low.

Exposure

Each PSG has two exposure timers. These timers can generate two periodic exposure output signals to control the exposure time and other external events related to the video source. Using auxiliary output signals, you can output either exposure signal in TTL or LVDS format.

The exposure timers can use a clock that is internally generated or one from an external source. In the latter case, you can define an auxiliary signal as the clock source (timer clock input).

Quadrature decoder

Each PSG features a quadrature decoder that can decode input from a rotary encoder with quadrature output. A rotary encoder (sometimes called a quadrature encoder) is a device that provides information about the position of a rotating shaft. The encoder outputs a two-bit code (also known as gray code) on two pairs of LVDS wires in a precise sequence: 00 01 11 10. The sequence determines the position of the rotating shaft and the direction of rotation.

The quadrature decoder can decode gray code and update a 16-bit internal counter. You can read the counter at different stages of the grab or trigger a grab based on the value of the counter. The quadrature decoder can support a maximum encoder frequency equal to the pixel clock frequency for the camera.

❖ You cannot power the rotary encoder using the Matrox Odyssey grab module; an external source must be used (for example, the computer's 5 V power source).

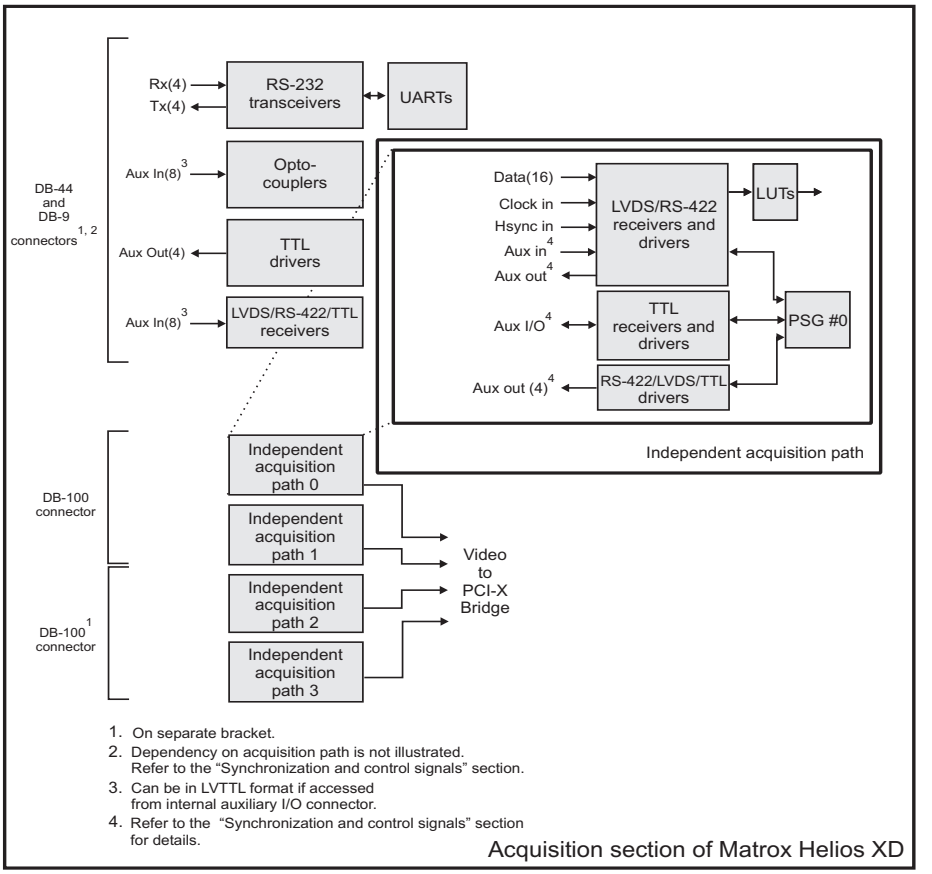
For each PSG, you can program two auxiliary signals as quadrature inputs. One to carry the first bit, and one to carry the second. Quadrature decoder settings can be toggled using **MdigControl**(), or by modifying the DCF file.

Matrox Helios XD acquisition section

Matrox Helios XD can capture video from LVDS or RS-422 digital video sources, depending on the version of the board purchased; unless otherwise specified, discussions of the LVDS version apply to the RS-422 version.

The board has four 16-bit acquisition paths that can be operated completely independently of each other. These paths can be configured to acquire from two, four, and eight-tap monochrome video sources, as well as from RGB video sources.

Each acquisition path can grab at a maximum rate of 60 MHz for LVDS and 32 MHz for RS-422. Each acquisition path has its own programmable synchronization generator (PSG) and LUTs, and can have a different acquisition rate. Matrox Helios XD supports a comprehensive set of general purpose I/O and serial ports to control video sources and other devices.



Performance

The video timing parameters supported by the board are as follows:

	Maximum
Number of pixels / line (including sync and blanking)	16 M
Number of lines / frame (including sync and blanking)	1 M
Pixel clock for LVDS	60 MHz
Pixel clock for RS-422	32 MHz
Bandwidth	480 Mbytes/sec for LVDS 256 Mbytes/sec for RS-422

Video sources supported

Matrox Helios XD has four, 16-bit, synchronous or asynchronous, digital acquisition paths. The following tables describe the video source combinations from which simultaneous, independent acquisition is supported and the acquisition paths (P#) to which they must be connected.

Configuration	Asynchronous video sources supported[1]			
	P0	P1	P2	P3
1	8-tap 8-bit monochrome, 4-tap 10-, 12-, 14-, 16-bit monochrome, or 10-, 12-, 14-, 16-bit RGB			
2	8-bit RGB or 2-tap 10-, 12-, 14-, 16-bit monochrome or 4-tap 8-bit monochrome		8-bit RGB or 2-tap 10-, 12-, 14-, 16-bit monochrome or 4-tap 8-bit monochrome	
3	8-bit RGB or 2-tap 10-, 12-, 14-, 16-bit monochrome or 4-tap 8-bit monochrome		1-tap 8-, 10-, 12-, 14-, 16-bit monochrome or 2-tap 8-bit monochrome	1-tap 8-, 10-, 12-, 14-, 16-bit monochrome or 2-tap 8-bit monochrome
4	1-tap 8-, 10-, 12-, 14-, 16-bit monochrome or 2-tap 8-bit monochrome	1-tap 8-, 10-, 12-, 14-, 16-bit monochrome or 2-tap 8-bit monochrome	8-bit RGB or 2-tap 10-, 12-, 14-, 16-bit monochrome or 4-tap 8-bit monochrome	
5	1-tap 8-, 10-, 12-, 14-, 16-bit monochrome or 2-tap 8-bit monochrome	1-tap 8-, 10-, 12-, 14-, 16-bit monochrome or 2-tap 8-bit monochrome	1-tap 8-, 10-, 12-, 14-, 16-bit monochrome or 2-tap 8-bit monochrome	1-tap 8-, 10-, 12-, 14-, 16-bit monochrome or 2-tap 8-bit monochrome

1. Note that taps expected to come from the same video source can also come from different video sources as long as they are synchronized (genlocked). In this case, the grabbed data is stored in separate color bands of the same buffer; the buffer can be in planar format.

Lookup tables

The board has four 256-entry 8-bit programmable lookup tables (LUTs) and four 4096-entry 8- or 16-bit LUTs.

The LUTs can be operated in the following configurations:

- 8 palettes of one, two, three, four, or eight 256-entry 8-bit LUTs.
- 4 palettes of one, two, three, or four 1024-entry 8- or 16-bit LUTs.
- 1 palette of one, two, three, or four 4096-entry 8- or 16-bit LUTs.

14- and 16-bit data by-pass the LUTs.

The LUTs are programmed using the MIL-Lite function **MdigLut**().

UARTs

For each acquisition path, the module supports an RS-232 compatible serial interface. Each interface is mapped as a COM port so that it can be accessed through the Win32 API. Each interface is comprised of both a transmit port and a receive port, permitting the interface to work in full-duplex mode. The interfaces are on External auxiliary I/O connector 0.

Each interface is controlled by a Universal Asynchronous Receiver-Transmitter (UART). The UART features independently programmable baud rates, supporting all standard baud rates from 300 baud up to 115200[1] baud. In addition, the UART has an internal 8-byte FIFO memory buffer, and can generate system level interrupts for both transmit and receive operations.

PSGs

Each acquisition path has its own programmable synchronization generator (PSG). The PSGs allow Matrox Helios XD to adapt to many video standards. The PSGs are responsible for managing all video timing, synchronization, trigger, exposure, and user-defined input and output signals.

Each PSG allows for independent acquisition from video sources. Therefore, Matrox Helios XD allows acquisition from four independent video sources.

Synchronization and control signals

The following tables summarize the synchronization, timing, and control signals supported by Matrox Helios XD. Most of these signals are available by defining auxiliary (general purpose) signals as such in the DCF. When an acquisition path supports several signals of a specific type, the tables identify the one to which an auxiliary signal can be defined. For example, for acquisition path 0, you can define P0_LVDS/TTL_AUX_OUT2 as exposure output 0 and P0_LVDS/TTL_AUX_OUT3 as exposure output 1.

Note that only the auxiliary signals of the first acquisition path used by a video source are available (for example, if grabbing 10-bit RGB, only the auxiliary signals for path 0 are available).

1. Note that the maximum baud rate is highly dependant on the amount of computer resources available.

You can set each LVDS/TTL signal individually to either LVDS or TTL format when accessed from the external auxiliary I/O connector 0 (DB-44) of the cable adapter board.

Type of signal	Path#	Max # signals[1]	LVDS aux. input[2]				LVDS/TTL aux. input[3]								Opto aux. input[4]								TTL aux. I/O[2]			
			P0_LVDS_AUX(VSYNC)_IN	P1_LVDS_AUX(VSYNC)_IN	P2_LVDS_AUX(VSYNC)_IN	P3_LVDS_AUX(VSYNC)_IN	LVDS/TTL_AUX(TRIG)_IN0	LVDS/TTL_AUX(TRIG)_IN1	LVDS/TTL_AUX(TRIG)_IN2	LVDS/TTL_AUX(TRIG)_IN3	LVDS/TTL_AUX(TRIG)_IN4	LVDS/TTL_AUX(TRIG)_IN5	LVDS/TTL_AUX(TRIG)_IN6	LVDS/TTL_AUX(TRIG)_IN7	P0_OPTO_AUX(TRIG)_IN0	P0_OPTO_AUX(TRIG)_IN1	P1_OPTO_AUX(TRIG)_IN0	P1_OPTO_AUX(TRIG)_IN1	P2_OPTO_AUX(TRIG)_IN0	P2_OPTO_AUX(TRIG)_IN1	P3_OPTO_AUX(TRIG)_IN0	P3_OPTO_AUX(TRIG)_IN1	P0_TTL_AUX(TRIG)_IO	P1_TTL_AUX(TRIG)_IO	P2_TTL_AUX(TRIG)_IO	P3_TTL_AUX(TRIG)_IO
Trigger input	0	4	0				2	3	2	3	2	3	2	3	0	1							1			
	1	4		0			2	3	2	3	2	3	2	3			0	1						1		
	2	4			0		2	3	2	3	2	3	2	3					0	1					1	
	3	4				0	2	3	2	3	2	3	2	3							0	1				1
Field polarity input	0	1						0																		
	1	1								0																
	2	1										0														
	3	1												0												
Data valid input	0	1					0																			
	1	1							0																	
	2	1									0															
	3	1											0													
Timer clock input	0	1						0																		
	1	1								0																
	2	1										0														
	3	1												0												

Type of signal	Path#	Max # signals[1]	LVDS aux. input[2]				LVDS/TTL aux. input[3]								Opto aux. input[4]								TTL aux. I/O[2]			
			P0_LVDS_AUX(VSYNC)_IN	P1_LVDS_AUX(VSYNC)_IN	P2_LVDS_AUX(VSYNC)_IN	P3_LVDS_AUX(VSYNC)_IN	LVDS/TTL_AUX(TRIG)_IN0	LVDS/TTL_AUX(TRIG)_IN1	LVDS/TTL_AUX(TRIG)_IN2	LVDS/TTL_AUX(TRIG)_IN3	LVDS/TTL_AUX(TRIG)_IN4	LVDS/TTL_AUX(TRIG)_IN5	LVDS/TTL_AUX(TRIG)_IN6	LVDS/TTL_AUX(TRIG)_IN7	P0_OPTO_AUX(TRIG)_IN0	P0_OPTO_AUX(TRIG)_IN1	P1_OPTO_AUX(TRIG)_IN0	P1_OPTO_AUX(TRIG)_IN1	P2_OPTO_AUX(TRIG)_IN0	P2_OPTO_AUX(TRIG)_IN1	P3_OPTO_AUX(TRIG)_IN0	P3_OPTO_AUX(TRIG)_IN1	P0_TTL_AUX(TRIG)_IO	P1_TTL_AUX(TRIG)_IO	P2_TTL_AUX(TRIG)_IO	P3_TTL_AUX(TRIG)_IO
Quadrature input[5]	0	1					0	1																		
	1	1							0	1																
	2	1									0	1														
	3	1											0	1												
User input	0	12	0				1	2	6	7	8	9	10	11	4	5							3			
	1	12		0			6	7	1	2	8	9	10	11			4	5						3		
	2	12			0		6	7	8	9	1	2	10	11					4	5					3	
	3	12				0	6	7	8	9	10	11	1	2							4	5				3

1. The maximum # for each signal type cannot always be attained. The actual maximum depends on whether the required auxiliary signals are available or have been defined as another type.
2. On the digital video input connectors (100-pin).
3. On external auxiliary I/O connector 0 (DB-44).
4. Signals ending with IN0 are on external auxiliary I/O connector 1 (DB-9), wherease signals ending with IN1 are on external auxiliary I/O connector 0 (DB-44).
5. Note that a rotary encoder with quadrature output transmits a two-bit code so table entries denote bit position.

Type of signal	Path#	Max # signals[1]	LVDS aux. output[2]				LVDS/TTL aux. output[2]														TTL aux. output[3]				TTL Aux. I/O[2]			
			P0_LVDS_AUX(CLK)_OUT	P1_LVDS_AUX(CLK)_OUT	P2_LVDS_AUX(CLK)_OUT	P3_LVDS_AUX(CLK)_OUT	P0_LVDS/TTL_AUX(HSYNC)_OUT0	P0_LVDS/TTL_AUX(VSYNC)_OUT1	P0_LVDS/TTL_AUX(EXP)_OUT2	P0_LVDS/TTL_AUX(EXP)_OUT3	P1_LVDS/TTL_AUX(HSYNC)_OUT0	P1_LVDS/TTL_AUX(VSYNC)_OUT1	P1_LVDS/TTL_AUX(EXP)_OUT2	P1_LVDS/TTL_AUX(EXP)_OUT3	P2_LVDS/TTL_AUX(HSYNC)_OUT0	P2_LVDS/TTL_AUX(VSYNC)_OUT1	P2_LVDS/TTL_AUX(EXP)_OUT2	P2_LVDS/TTL_AUX(EXP)_OUT3	P3_LVDS/TTL_AUX(HSYNC)_OUT0	P3_LVDS/TTL_AUX(VSYNC)_OUT1	P3_LVDS/TTL_AUX(EXP)_OUT2	P3_LVDS/TTL_AUX(EXP)_OUT3	P0_TTL_AUX(EXP)_OUT	P1_TTL_AUX(EXP)_OUT	P2_TTL_AUX(EXP)_OUT	P3_TTL_AUX(EXP)_OUT	P0_TTL_AUX(TRIG)_IO	P1_TTL_AUX(TRIG)_IO	P2_TTL_AUX(TRIG)_IO	P3_TTL_AUX(TRIG)_IO
Exposure output	0	2							0	1													0							
	1	2											0	1										0						
	2	2															0	1							0					
	3	2																			0	1				0				
User output	0	7	0				1	2	3	4													6				5			
	1	7		0							1	2	3	4										6				5		
	2	7			0										1	2	3	4							6				5	
	3	7				0													1	2	3	4				6				5

1. The maximum # for each signal type cannot always be attained. The actual maximum depends on whether the required auxiliary signals are available or have been defined as another type.
2. On the digital video input connectors (100-pin).
3. On external auxiliary I/O connector 0 (DB-44).

Type of signal	Path#	Max # signals[1]	LVDS dedicated input signals[2 3]	LVDS aux. input[3]				LVDS/TTL aux. output[3]														LVDS aux. output[3]			
				P0_LVDS_AUX(VSYNC)_IN	P1_LVDS_AUX(VSYNC)_IN	P2_LVDS_AUX(VSYNC)_IN	P3_LVDS_AUX(VSYNC)_IN	P0_LVDS/TTL_AUX(HSYNC)_OUT0	P0_LVDS/TTL_AUX(VSYNC)_OUT1	P0_LVDS/TTL_AUX(EXP)_OUT2	P0_LVDS/TTL_AUX(EXP)_OUT3	P1_LVDS/TTL_AUX(HSYNC)_OUT0	P1_LVDS/TTL_AUX(VSYNC)_OUT1	P1_LVDS/TTL_AUX(EXP)_OUT2	P1_LVDS/TTL_AUX(EXP)_OUT3	P2_LVDS/TTL_AUX(HSYNC)_OUT0	P2_LVDS/TTL_AUX(VSYNC)_OUT1	P2_LVDS/TTL_AUX(EXP)_OUT2	P2_LVDS/TTL_AUX(EXP)_OUT3	P3_LVDS/TTL_AUX(HSYNC)_OUT0	P3_LVDS/TTL_AUX(VSYNC)_OUT1	P3_LVDS/TTL_AUX(EXP)_OUT2	P3_LVDS/TTL_AUX(EXP)_OUT3	P0_LVDS_AUX(CLK)_OUT	P1_LVDS_AUX(CLK)_OUT	P2_LVDS_AUX(CLK)_OUT	P3_LVDS_AUX(CLK)_OUT
VSYNC	0	1 in+ 1 out		in					out																
	1	1 in+ 1 out			in								out												
	2	1 in+ 1 out				in												out							
	3	1 in+ 1 out					in															out				
HSYNC	0	1 in+ 1 out	P0_LVDS_HSYNC_IN					out																		
	1	1 in+ 1 out	P1_LVDS_HSYNC_IN									out														
	2	1 in+ 1 out	P2_LVDS_HSYNC_IN													out										
	3	1 in+ 1 out	P3_LVDS_HSYNC_IN																		out					
Clock	0	1 in+ 1 out	P0_LVDS_CLK_IN																					out			
	1	1 in+ 1 out	P1_LVDS_CLK_IN																						out		
	2	1 in+ 1 out	P2_LVDS_CLK_IN																							out	
	3	1 in+ 1 out	P3_LVDS_CLK_IN																								out

1. The maximum # for each signal type cannot always be attained. The actual maximum depends on whether the required auxiliary signals are available or have been defined as another type.
2. In this column, each signal is a dedicated signal (that is, it cannot be redefined as another type of signal); therefore these signals are always available. These signals are received on/transmitted from the digital video input connectors (100-pin).
3. On the digital video input connectors (100-pin).

Auxiliary signals

The board supports auxiliary multi-purpose input and output signals. Auxiliary input signals can be routed as trigger input (for example, to synchronize image acquisition with external events), quadrature input, field polarity, data valid, timer clock input, or user-defined signals (for example, to synchronize an application with a user-defined event). Auxiliary output signals can be routed as exposure signals or user-defined signals (for controlling external devices, such as a strobe light or programmable logic controller).

The board supports auxiliary signals in different formats:

Auxiliary signals	# per path	# total
Auxiliary input signals that can be defined as either TTL or LVDS.	depends on type of signal	8
Opto-isolated auxiliary input signals.	2	8
LVDS auxiliary input signals.	1	4
TTL auxiliary signals that can be defined as either input or output.	1	4
Auxiliary output signals that can be defined as either TTL or LVDS.	4	16
LVDS auxiliary output signals.	1	4
TTL auxiliary output signals.	1	4

Note that the opto-isolated signals pass through an opto-coupler, a device that protects the board from outside surges and different ground levels, and permits total electrical isolation from the frame grabber.

You specify the purpose of the auxiliary signals in the DCF. You can then program these signals using the MIL-Lite function **MdigControl**() with M_USER..., M_TRIGGER..., or M_GRAB_EXPOSURE....

Synchronization

Each PSG can accept and/or provide one horizontal (HSYNC) and one vertical (VSYNC) synchronization signal (slave or master mode).

With interlaced video sources, you can typically establish which field is being input by noting the phase shift between the horizontal and the vertical synchronization signals. Alternatively, you can define an auxiliary signal as a field polarity input signal and transmit the field polarity on this signal.

To establish which pixels are active in a line (because the horizontal synchronization signal does not identify the blanking portion of the signal), the board can generate a data valid signal based on information specified in the DCF. Alternatively, you can define an auxiliary input signal as a data valid signal.

Clock

Each PSG can accept or provide one pixel clock signal (slave or master mode).

Trigger signals

Each PSG accepts two external trigger inputs: one TTL or opto-isolated trigger input and another LVDS or opto-isolated trigger input. For each PSG, you can also program two path-independent auxiliary signals as trigger inputs; these can be received in LVDS or TTL.

Each PSG can operate in one of the two following trigger modes; the mode is specified by the DCF:

- **Next valid frame/field mode.** In this mode, the board waits for the next valid frame or field (as specified by the DCF file) before commencing the grab. This trigger mode functions in one of three ways:
  - **Edge-triggered monoshot acquisition.** The board waits for the rising/falling edge to capture a single frame.
  - **Edge-triggered continuous acquisition.** The board waits for the rising/falling edge to start a continous grab.
  - **Level-sensitive continuous acquisition.** The board grabs continuously while the level of the trigger is high/low.
  - ❖ The polarity of the active and inactive levels of the trigger signal is software programmable.
- **Asynchronous reset mode.** In this mode, the board resets the video source to begin a new frame when the trigger signal is received.

Trigger format

When received in TTL format directly, the signal must have a maximum amplitude of 5 V. A signal over 2 V is considered high, while anything less than 0.8 V is considered low; the transition of 0.8 V to 2 V is considered to be the rising edge.

If using the trigger to start acquisition, the trigger signal's pulse width must be greater than two pixels; if using the trigger to start the exposure timer, the trigger signal's pulse width must be greater than two clock periods of the timer. To determine the timer period, take the inverse of the pixel or timer's clock frequency, respectively. For example, if the pixel frequency is 12.27 MHz, the minimum pulse width is 2 x 1/12.27 MHz (approximately 164 nsec).

The opto-isolated trigger signals pass through an opto-coupler. The voltage difference across the positive and negative components of the signal must be between 4.06 V and 9.165 V for logic high, and between -5.0 V and 0.8 V for logic low.

Exposure

Each PSG has two exposure timers. These timers can generate two periodic exposure output signals to control the exposure time and other external events related to the video source. Using auxiliary output signals, you can output both exposure signals in TTL or LVDS format.

The timers can use a clock that is internally generated or one from an external source. In the latter case, you can define an auxiliary signal as the clock source (timer clock input).

Quadrature decoder

Each PSG features a quadrature decoder that can decode input from a rotary encoder with quadrature output. A rotary encoder (sometimes called a quadrature encoder) is a device that provides information about the position of a rotating shaft. The encoder outputs a two-bit code (also known as gray code) on two pairs of LVDS wires in a precise sequence: 00 01 11 10. The sequence determines the position of the rotating shaft and the direction of rotation.

The quadrature decoder can decode gray code and update a 16-bit internal counter. You can read the counter at different stages of the grab or trigger a grab based on the value of the counter. The quadrature decoder can support a maximum encoder frequency equal to the pixel clock frequency for the camera.

❖ You cannot power the rotary encoder using the Matrox Odyssey grab module; an external source must be used (for example, the computer's 5 V power source).

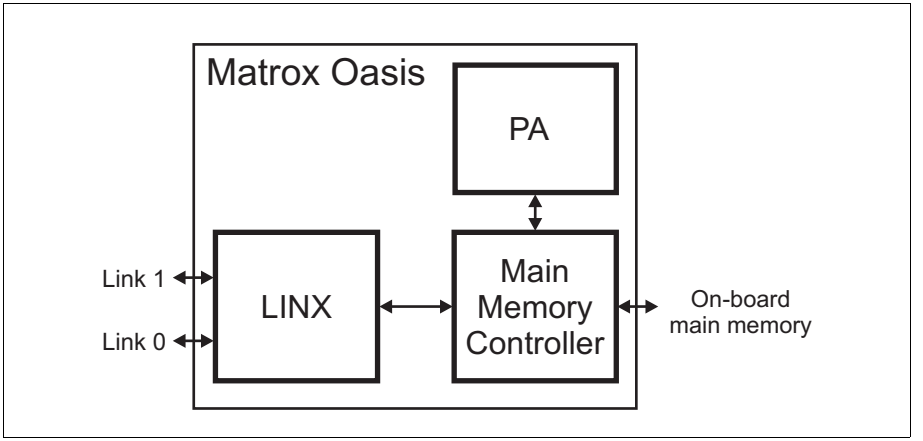
For each PSG, you can program two auxiliary signals as quadrature inputs. One to carry the first bit, and one to carry the second. Quadrature decoder settings can be toggled using **MdigControl**(), or by modifying the DCF file.

Matrox Oasis

To alleviate the Host CPU from image formatting and preprocessing tasks, both Matrox Helios XCL and XA include the custom Matrox Oasis ASIC. Matrox Oasis is a high-density chip that combines a powerful processing core and a PCI-X controller.

Matrox Oasis allows processing to be independent of the grab, so you can perform flexible, real-time operations. For example, you can double-buffer by alternating the grab between two destination buffers.

The Matrox Oasis ASIC features a main memory controller to interface with on-board main memory (DDR SDRAM), a links controller (LINX) with two ports (Oasis link ports) that can handle streams of data and can format them, and a pixel accelerator (PA) for preprocessing. This section discusses each of these features in turn.

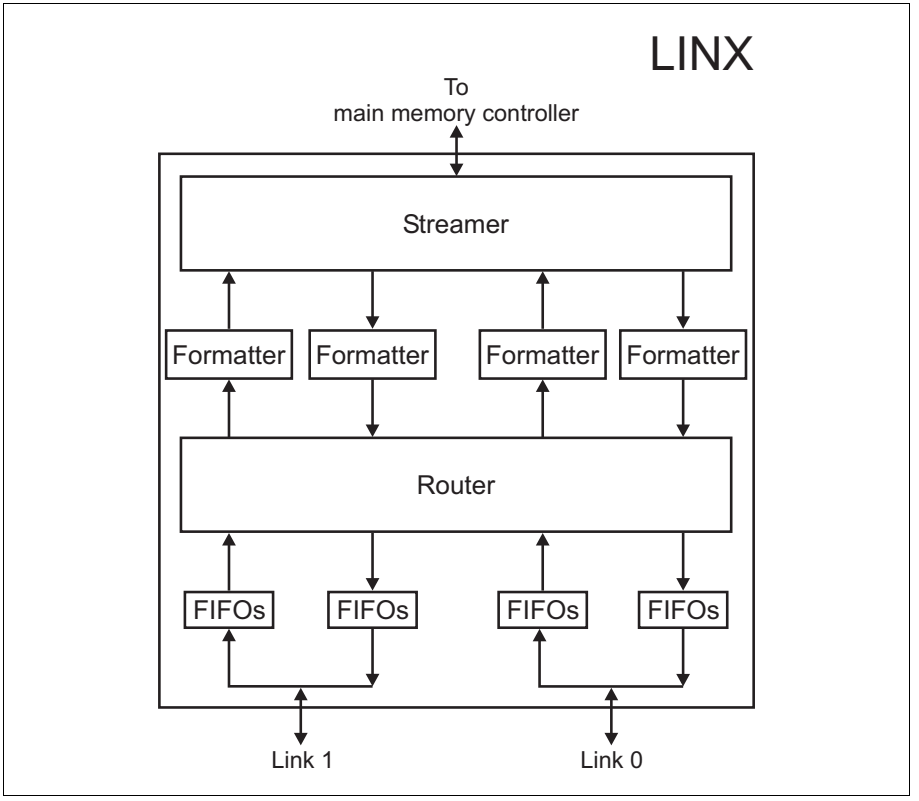


Memory controller

Matrox Oasis includes a very efficient main memory controller for managing the DDR 128-bit wide interface to on-board main memory (DDR SDRAM). Operating at 133 MHz, the DDR SDRAM memory and controller combine to deliver a memory bandwidth in excess of 4 Gbytes/sec. This memory bandwidth allows Matrox Helios to comfortably handle demanding video I/O while maintaining PA performance.

Links controller

The links controller (LINX) is the router that manages all data movement inside and outside Matrox Oasis. The LINX can receive video data in stream format from an Oasis link port, and then write it to memory through the main memory controller. When the data is received in stream format, the video stream is known as an input stream. The LINX can read sequential data from memory and transmit it through an Oasis link port using PCI addressing. This is known as an output stream.



Video streams are used to transfer image data from the acquisition section to Matrox Oasis.

Each video stream can transfer images with the following maximum dimensions. Multiple video streams can be used to support even more demanding applications.

Dimension	Maximum
Image size (pixel resolution)	16 Mpixels wide and 1 Mpixels in height
Number of components (taps or bands)	up to 4
Number of bits/component	8 or 16

The LINX can simultaneously manage:

- Up to 64 video input data streams that have different destinations.
- Two video output streams.

Matrox Oasis can generate interrupts at the start and end of a video stream transfer, as well as at the end of a specific line within a frame.

Each Oasis link port can operate in a different mode and clock frequency. Slow targets can regulate the pace of the video stream that they are receiving so that excess Oasis link port bandwidth is not lost.

Formatters

The formatters can perform the following on the video streams:

- Source and destination alignments (with pixel resolution).
- Plane (component) separation on input streams and merging on output streams.
- Input cropping (also known as input windowing). This allows you to extract a region of interest (with pixel resolution) from an input stream.
- Horizontal sub-sampling of input and output streams. Integer subsampling factors from 1 to 16 are supported. (The formatters are not required for vertical subsampling; this is handled directly by the memory controller.)
- Independent control of horizontal scanning direction for input streams. The formatters are not required to control the vertical scan direction; this is handled directly by the memory controller. Control over the scan direction is particularly useful for reconstructing a proper image from a video source that uses multiple taps, each with different scanning directions.

The formatters manipulate the data of an input stream only if it is being written to memory (through the main memory controller). In addition, any available formatter can be used on an input video stream.

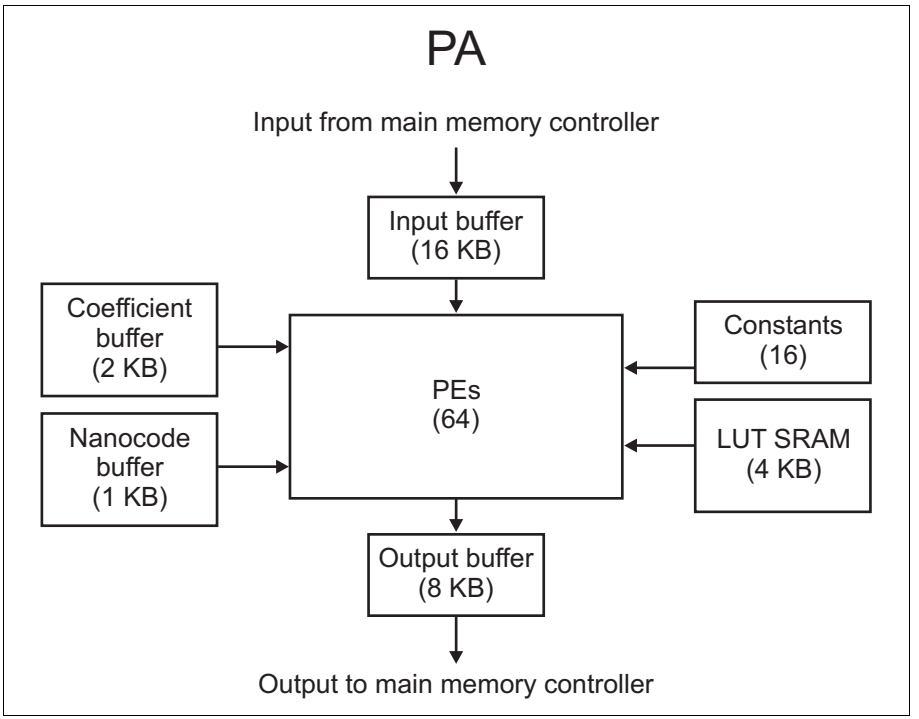
Note that input cropping and subsampling are applied in parallel to all components of a stream.

Router

The router is responsible for routing streams to the appropriate destination; it uses a routing table to determine how streams travel through the router. The router arbitrates between multiple streams and PCI transactions that have the same destination, based on their priority level; real-time video streams are assigned the highest priority.

Pixel Accelerator

The pixel accelerator (PA), integrated in the Matrox Oasis ASIC, is designed for calculation-intensive image preprocessing. It is very efficient at performing most neighborhood, point-to-point, and LUT mapping operations.



The PA can accept up to four source buffers and output to four destination buffers, allowing several operations to be performed at once in a single pass (for example, four images can be averaged in one pass).

The PA supports 1-, 8-, and 16- data types. For point-to-point operations, it also supports 32-bit data types.

The PA operates at a core frequency of 133 MHz, for a peak processing power of 100 billion operations per second (BOPS). With a peak memory bandwidth of up to 4.3 Gbytes/sec, the PA can process over 2 billion 8-bit pixels/sec and reduce the time required by I/O-intensive operations.

Input and output

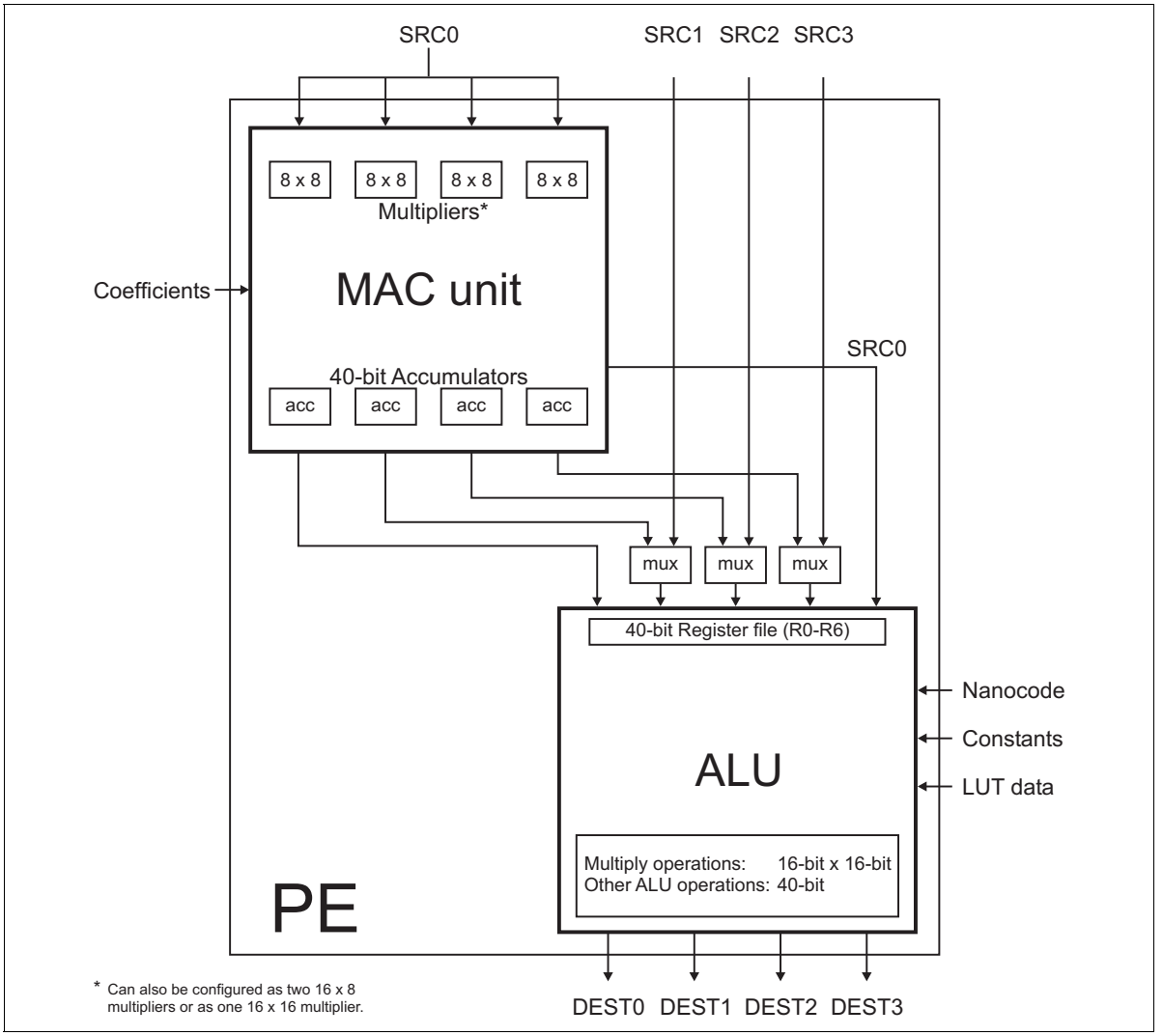
Instead of randomly accessing data in memory, the PA is programmed to stream data from one to four rectangular regions of memory (image buffers) and to process the data with many processing elements (PE) operating in parallel. Once the PA is programmed with the location of the input and output images, as well as the operations to be performed, a processing pass is started, and the PA operates completely autonomously until it has finished.

The PA addresses external memory through the memory controller. This interface is identical to the other read/write ports of the memory controller, except that one read and one write request can be sent to the memory controller instead of a single read or write. The memory controller acts as a slave upon memory access requests from the PA.

The PA efficiently fetches from memory all rows of image data (from the different sources) required to process one or more rows of the source images, and stores this data in the PA's 16 Kbyte input buffer. For very wide images, the PA processes the images in wide vertical strips.

PEs

The PA has 64 processing elements (PEs) that work in parallel. Each PE has the following structure:



The PEs operate as a linear array, whereby each consecutive PE works on a horizontally adjacent result pixel. When performing a neighborhood operation, each PE can sometimes work on two 16-bit or four 8-bit result pixels at a time; this is referred to as operating in dual and quad pixel mode, respectively. In addition, each PE can process 32 packed binary pixels at time.

To maximize efficiency on all image widths (so that all PEs are fully utilized), the PA can split the PE linear array into shorter segments, each responsible for a different horizontal strip (set of rows) of the source image. The segments can be a power of two in length, from 32 to 256 pixels.

MAC unit

The main function of the MAC unit is to perform one (and only one at a time) of the following operations:

- Convolution.
- Grayscale morphology.
- Binary morphology.
- 3×3 connectivity mapping (for fast binary thinning).
- Vector product (for color conversion).

Point-to-point operations don't use the MAC unit (except as a pass through when they use all four sources); they only use the ALU.

The MAC unit is capable of performing a single 16-bit by 16-bit, two 8-bit by 16-bit, or four 8-bit by 8-bit multiplies with 40-bit accumulation per cycle for convolution operations. In the latter case, this represents 42 GigaMACs/sec. The 40-bit accumulator guarantees no overflow situation for a 16 by 16 kernel with 16-bit coefficients and data. In addition, the PA architecture allows symmetrical kernels to be processed up to four times faster. A kernel is symmetric if one half of it (either horizontally or vertically) is a mirror image of the other half.

The MAC unit is also able to perform up to four minimum or maximum operations per cycle for grayscale morphology operations.

Only one source can be fed to the MAC unit, and the supported data types are 1-bit for binary morphology and 3×3 connectivity mapping, and 8- and 16-bit for the other operations. In single pixel mode, the MAC unit produces a single result to be transferred to the ALU per output pixel. However, depending on the data type, dual or quad pixel modes can be used, which produce, respectively, two or four results to be transferred to the ALU at a time. If needed, the MAC unit

can also pass the original source pixel (the centre pixel of the neighborhood) to the ALU along with the accumulated results. Therefore, a maximum of five values can be transferred from the MAC unit to the ALU for each pixel.

The maximum number of kernel elements is 1024 if they are 16-bit, 2048 if they are 8-bit, or 8192 for binary morphology (stored as 2 bits per element, where one bit is a *don't care* mask). This represents, for example, a 32x32 16-bit kernel, a 45x45 8-bit kernel, or a 90x90 1-bit kernel. However, symmetrical 8- or 16-bit kernels can be larger than this because not all kernel elements need to be used in this case.

The PA can perform a convolution with up to four kernels at the same time, subject to the following restrictions:

- All kernels must have the same size, centre, data type, and symmetry.
- All kernels are applied to the same source image.

The PA can perform grayscale morphology with up to two kernels (structuring elements), but there are some differences from convolution with multiple kernels. The rules for grayscale morphology with two kernels are:

- Both kernels must have the same size, centre, and symmetry.
- Both kernels are applied to the same source image.
- The first kernel always performs a MIN operation (erosion).
- The second kernel always performs a MAX operation (dilation).

Multiple kernels are not supported for binary morphology.

ALU

The ALU is 40 bits wide and can execute a wide variety of arithmetic and logical operations. It can be programmed to execute a sequence of up to 256 instructions per pixel at one instruction per clock cycle. This allows complex sequences of I/O bound operations to be combined into a single processing pass, reducing the amount of memory accesses and further improving performance.

For each pixel, up to five values (MAC results or point sources) can be transferred to the register file of the ALU, into the first five of the seven 40-bit registers. Registers that are not needed to hold MAC results or point sources can be used to accumulate results during a processing pass, and any of them can be used to hold intermediate values temporarily during a single sequence of instructions.

The ALU also has sixteen 40-bit constant registers, which are pre-loaded at the beginning of a processing pass with values needed by the instruction sequence.

On each clock cycle, the ALU can execute an instruction that operates on one or two operands. The operands can be:

- A register from the register file.
- A constant register.
- The result of an ALU operation (except for multiply) from one or two instructions before.
- The result of a multiply operation from two or three instructions before.

The ALU can perform one of the following instructions: absolute value, clip, shift, add, subtract, multiply, minimum, maximum, logical AND, logical OR, logical XOR, logical NOT, or LUT map. It can also perform other more specialized operations. Note that all instructions can work on 40 bits, except multiply instructions which work on 16 bits (producing a 32-bit result).

Lookup tables

The hardware provides direct support in the ALU for LUTs with a size of 256 bits. This is enough to implement an 8-in:1-out, 7-in:2-out, 6-in:4-out, or 5-in:8-out LUT in a single instruction. Using multiple 8-in:1-out LUT mapping instructions (which can shift and merge mapping results with the result of the previous LUT instruction), the ALU can perform a very fast 256 entry 8-bit LUT mapping. Even larger LUT mappings can be constructed out of a combination of basic LUT instructions; however, the larger the LUT, the slower the operation.

Memory

Matrox Helios supports up to 256 Mbytes of linearly addressable, DDR SDRAM main memory (also referred to as processing memory). Main memory is accessed through Matrox Oasis. Matrox Oasis has a 133 MHz 128-bit DDR interface to main memory, for data transfers at a rate of up to 4.3 Gbytes/sec. Main memory holds image and post-processing result data.

By default, some main memory is mapped onto the PCI bus so that you can use a Host pointer to access this memory, or you can access it directly from another PCI/PCI-X bus master; this memory is referred to as shared memory. To allocate a buffer in shared memory, use the MIL-Lite function **MbufAlloc...**() with **M_SHARED**. To increase or decrease the amount of shared memory, use the MIL Configuration utility. If your application accesses multiple boards that have their memory mapped onto the PCI bus, ensure that the total amount of memory mapped onto the PCI bus does not exceed the maximum address space available to your application.

PCI/PCI-X interface

Matrox Helios is a PCI-X board. PCI-X is a high-performance backwards-compatible enhancement to the conventional PCI bus specification. As such, Matrox Helios can transfer data using either the Host's PCI bus or PCI-X bus, depending on the slot used by the board.

On Matrox Helios XCL and XA, a standard PCI-X to PCI-X bridge handles the PCI/PCI-X connections.

Using the Host PCI/PCI-X bus, Matrox Helios can copy data between its main memory, the Host, and any other memory mapped onto the PCI/PCI-X bus. The PCI/PCI-X bus connects all Matrox Helios components to the Host, and to peripherals such as a display board.

Matrox Helios can exchange data with the Host at a peak of up to 1 Gbyte/sec when used with a PCI-X slot. Matrox Helios can also be used with a conventional 3.3 or 5 V[1] PCI slot, in which case the maximum transfer rate is reduced (132 Mbytes/sec for a 33 MHz 32-bit PCI slot, 266 Mbytes/sec for a 66 MHz 32-bit PCI slot, 532 Mbytes for a 66 MHz 64-bit PCI slot).

Using the PCI/PCI-X bus, Matrox Helios can also access Host DMA memory (physically contiguous, non-paged memory). An advantage of DMA memory is that a bus mastering device (such as Matrox Helios) can access this memory without the help of the Host CPU.

As previously mentioned, you can also map some Matrox Helios main memory onto the PCI bus so that you can use a Host pointer to access this memory, or you can access it directly from another PCI/PCI-X bus master.

Watchdog circuitry

Matrox Helios XCL, XA and XD all have Watchdog circuitry[1] to automatically recover from application or system failure. The Watchdog circuitry automatically reboots your computer when, for some reason, your computer hangs for longer than a pre-set amount of time.

The Watchdog circuitry works based on an integrated timer. When the Watchdog circuitry is enabled, it must receive a reset signal ("pulse") from an application or from the Matrox Helios driver within the time specified by the timer. Every time the signal is received, Watchdog resets its timer. If, however, the Watchdog circuitry does not receive a signal for a period longer than the time allotted by the timer, it will send a hardware reset signal to reboot the computer.

You can enable the Watchdog circuitry, set the Watchdog timer, and send a reset signal using the MIL-Lite **MsysControl**() function.

Flash EEPROM

Matrox Helios XCL, XA and XD all have an 8-Mbyte flash EEPROM. It stores:

- Board initialization parameters and board data.
- Configuration data for the acquisition section.

1. 5 V starting from revision 1 of the Matrox Helios PCB; revision 0 is only 3.3 V PCI tolerant.
1. Starting from revision 1 of the Matrox Helios XCL PCB; whereas, present on the Matrox Helios XA PCB as of revision 0.

Appendix A: Glossary

This appendix defines some of the specialized terms used in the Matrox Helios documentation.

- ***ASIC***

  Application-specific integrated circuit. A custom-made integrated circuit made to meet the requirements of a specific application by integrating several digital and/or analog functions into a single die. Integrating the functions into a single die results in a reduction in cost, board area, and power consumption, while improving performance when compared to an equivalent implementation using off-the-shelf components.

- ***Bandwidth***

  A term describing the capacity to transfer data. Greater bandwidth is needed to sustain a higher transfer rate. Greater bandwidth can be achieved, for example, by using a wider bus.

- ***Blanking period***

  The portion of a video signal after the end of a line or frame, and before the beginning of a new line or frame. During this period, the video signal is "blank" so that a scan line can be brought back to the beginning of the new line or frame. The portion of a video signal after the end of a line and before the beginning of a new line is known as the *horizontal blanking period*. The portion of a video signal after the end of a frame and before the beginning of a new frame is known as the *vertical blanking period*.

- ***Contiguous memory***

  A block of memory occupying a single, unbroken series of addresses.

- ***DCF***

  Digitizer Configuration Format. A file format that defines the input data format and, for example, how to accept or generate video timing signals such as horizontal sync, vertical sync, and pixel clock.

  Such files have a *.dcf* extension.

- ***DDR SDRAM***

  Double Data Rate Synchronous Dynamic Random Access Memory. A type of memory used for processing. SDRAM allows the Matrox Helios to access data as fast as possible, which is important for I/O-bound functions.

- ***Digitizer Configuration Format***

  See DCF.

- ***Double buffering***

  Alternating the destination of an operation between two buffers. Double buffering allows you to, for example, process one buffer while grabbing into the other buffer.

- ***Dynamic range***

  The range of values present in a buffer. An unsigned 8-bit buffer, for example, has an allowable range of 0 to 255; its dynamic range can be any range within these values.

- ***Exposure signal***

  The signal generated by one of the programmable timers of the frame grabber module. The exposure signal can be used to control external hardware. For example, it can be fed to the video source to control its exposure time or used to fire a strobe light.

- ***Exposure time***

  Refers to the period during which the image sensor of a video source is exposed to light. As the length of this period increases, so does the image brightness.

- ***Field***

  One of the two halves that together make up the image grabbed from an interlaced video source. One half consists of the image's odd lines (known as the *odd field*); the other half consists of the image's even lines (known as the *even field*).

- ***Frame***

  A single image grabbed from a video source.

- ***Gain level***

  The factor by which an analog input signal is scaled. The gain affects the brightness and contrast of the resulting image.

- ***Grab***

  To acquire an image from a video source.

- ***Horizontal blanking period***

  The portion of a video signal after the end of a line and before the beginning of a new line. During this period, the video signal is "blank".

  See also *vertical blanking period*.

- ***Horizontal synchronization signal***

  The part of a video signal that indicates the end of a line and the start of a new one.

  See also *vertical synchronization signal*.

- ***Interlaced scanning***

  Describes a transfer of data in which the odd-numbered lines of the source are written to the destination buffer first, and then the even-numbered lines (or vice-versa).

  See also *progressive scanning*.

- ***Latency***

  The time from when an operation is started to when the final result is produced.

- ***LUT mapping***

  Lookup table mapping. A point-to-point operation that uses a table to define a replacement value for each possible pixel value in an image.

- ***LVDS***

  Low-voltage differential signalling. LVDS offers a general-purpose, high bandwidth interface standard for serial and parallel data interfaces that require increased bandwidth at high speed, with low noise and power consumption.

- ***Progressive scanning***

  Describes a transfer of data in which the lines of the source are written sequentially into the destination buffer.

  See also *interlaced scanning*.

- ***Real-time processing***

  The processing of an image as quickly as the next image is grabbed.

  Also known as *live processing*.

- ***Reference levels***

  The zero and full-scale levels of an analog-to-digital converter. Voltages below a *black reference level* are converted to a zero pixel value; voltages above a *white reference level* are converted to the maximum pixel value. Together with the analog gain factor, the reference levels affect the brightness and contrast of the resulting image.

- ***Saturate***

  To replace overflows (or underflows) in an operation with the highest (or lowest) possible value that can be held in the destination buffer of the operation.

- ***Stream***

  The communication path through which nodes can transmit data.

- ***UART***

  Universal Asynchronous Receiver/Transmitter. A component that handles asynchronous communication through an RS-232 serial interface.

- ***Vertical blanking period***

  The portion of a video signal after the end of a frame and before the beginning of a new frame. During this period, the video signal is "blank".

  See also *horizontal blanking period*.

- ***Vertical synchronization signal***

  The part of a video signal that indicates the end of a frame and the start of a new one.

  See also *horizontal synchronization signal*.

Appendix B: Technical information

This appendix contains information that might be useful when installing your Matrox Helios board.

Board summary

Global information

- Operating system: See your software manual for supported versions of Microsoft Windows.

- Computer requirements:

  - An available conventional PCI slot or a PCI-X slot.

  - Processor with an Intel 32-bit architecture (IA32) or equivalent.

  - A relatively up-to-date PCI/PCI-X chipset, such as the Intel E7500 series, ServerWorks (HE, LE, LC, or HE SL), or ServerWorks GC (HE, LE, WS, or SL).

Important

  - A proper power supply and proper ventilation. Refer to the *Electrical specifications* and *Ventilation requirements* sections, respectively.

  Matrox does not guarantee compatibility with all computers that have the above specifications. Please consult with your local Matrox Imaging representative, local Matrox Imaging sales office, or the Matrox Imaging Customer Support Group at headquarters before using a specific computer.

Technical features of Matrox Helios XCL

- Two factory configured versions:

  - Two independent Camera Link Base acquisition paths (dual-Base).

  - Single Camera Link Base/Medium/Full acquisition path (single-Full).

- PCI/PCI-X short board with a universal (3.3 V - 5 V) 64-bit board edge connector (5 V starting from revision 1 of the Matrox Helios PCB; revision 0 is only 3.3 V PCI tolerant).

- ChannelLink speed of up to 85 MHz.

- Supports frame and line-scan video sources.

- Four 256 entry 8-bit LUTs and four 4096 entry 8-bit or 16-bit LUTs. (14 and 16-bit data by-pass the LUTs).
- 128/256 Mbytes of 133 MHz DDR SDRAM main memory. Over 4.3 Gbytes/sec of memory bandwidth.
- Six TTL configurable auxiliary I/Os (trigger, field polarity, timer clock, or user input, or exposure or user output). See the *Matrox Helios hardware reference* chapter for supported configurations.
- Four LVDS configurable auxiliary inputs (trigger, field polarity, timer clock, synchronization, or user input). See the *Matrox Helios hardware reference* chapter for supported configurations.
- Four LVDS configurable auxiliary outputs (exposure or user output). See the *Matrox Helios hardware reference* chapter for supported configurations.
- Two LVDS serial ports (dual-Base version), one LVDS serial port (single-Full version).
- Two separate LVDS pixel clock, HSYNC and VSYNC outputs.
- Four opto-isolated configurable auxiliary inputs.
- Internal video generator for diagnostics.
- 8 Mbytes flash EEPROM.
  - Note that EEPROM is limited to 10000 write cycles.
- Supports a 64-bit 66/100/133 MHz 3.3 V PCI-X (or a 64-bit 33/66 MHz 3.3 V or 5 V conventional PCI) Host interface.
- Integrated Watchdog circuitry[1] for automatically recovering from application or system failure.
- Supports an external rotary encoder with quadrature output.

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1. Starting from revision 1 of the Matrox Helios XCL PCB.

Technical features of Matrox Helios XA

- PCI/PCI-X long board with a universal (3.3 V - 5 V) 64-bit board edge connector (5 V starting from revision 1 of the Matrox Helios PCB; revision 0 is only 3.3 V PCI tolerant).

- Four independant acquisition paths. Each acquisition path has the following:

  - Input from one of two software selectable sources. The source can be either AC or DC coupled.

  - Two low-pass filters: a 40 MHz filter and a 7.5 MHz filter.

  - Variable gain amplifier and adjustable offset to set the black and white reference levels.

  - 10-bit A/D, with a sampling rate of up to 80 MHz.

- Four 4096 entry 8- or 16-bit programmable LUTs.

- Acquisition paths can be combined to acquire from:

  - Component RGB video source.

  - Two dual-tap monochrome video sources.

  - Two monochrome video sources at up to 160 Msamples/sec.

- Supports frame and line-scan video sources.

- Four PSGs. For each PSG, there is the following:

  - Adjustable clock phase (256 steps with 0.5 ns resolution).

  - LVDS/TTL pixel clock, HSYNC, and VSYNC inputs or outputs.

  - A TTL auxiliary input (trigger, field polarity, or user input).

  - A TTL auxiliary output (exposure or user output).

  - An opto-isolated auxiliary input (trigger or user input).

  - RS-232 serial port.

  - Status LED.

- 128/256 Mbytes of 133 MHz DDR SDRAM main memory. Over 4.3 Gbytes/sec of memory bandwidth.

- Eight TTL/LVDS configurable auxiliary inputs (trigger, field polarity, data valid, timer clock, synchronization, and/or user input). See the *Matrox Helios hardware reference* chapter for supported configurations.

- Eight TTL/LVDS configurable auxiliary outputs (exposure, synchronization, or user output). See the *Matrox Helios hardware reference* chapter for supported configurations.

- Internal video generator for diagnostics.

- 8 Mbytes flash EEPROM.

  ❖ Note that EEPROM is limited to 10000 write cycles.

- Supports a 64-bit 66/100/133 MHz 3.3 V PCI-X (or a 64-bit 33/66 MHz 3.3 V or 5 V conventional PCI) Host interface.

- Integrated Watchdog circuitry for automatically recovering from application or system failure.

- Supports an external rotary encoder with quadrature output.

Technical features of Matrox Helios XD

- PCI/PCI-X long board with a universal (3.3 V - 5 V) 64-bit board edge connector.

- Four independent acquisition paths. Each acquisition path supports the following:

  - 16-bit wide LVDS or RS-422 interface.

  - Acquisition rates up to 60 MHz for LVDS and 32 MHz for RS-422.

  - LVDS/RS-422 vsync/auxiliary, hsync, and clock inputs.

  - Five LVDS/RS-422 configurable auxiliary outputs (exposure, synchronization, clock, or user output). Four of these outputs can be TTL.
  - Two opto-isolated configurable auxiliary inputs (trigger or user input).
  - One TTL configurable auxiliary I/O (trigger input 1, user input, or user output).
  - One TTL configurable auxiliary output (exposure or user output).
  - Serial communication port.

- Acquisition paths can be combined to acquire from:
  - Four single-tap 8 to 16-bit or dual-tap 8-bit monochrome sources.
  - Two dual-tap 10 to 16-bit or four-tap 8-bit monochrome sources.
  - One four-tap 10 to 16-bit or eight-tap 8-bit monochrome source.
  - Two 8-bit RGB sources.
  - One 10 to 16-bit RGB source.
- Four 256-entry 8-bit programmable lookup tables (LUTs) and four 4096 entry 8- or 16-bit LUTs.
- Supports frame and line-scan video sources.
- 256 Mbytes of 133 MHz DDR SDRAM main memory. Over 4.3 Gbytes/sec of memory bandwidth.
- Eight LVDS/RS-422 configurable auxiliary inputs (trigger, field polarity, data valid, timer clock, and/or user input). All can be TTL. See the *Matrox Helios hardware reference* chapter for supported configurations.
- Internal video generator for diagnostics.

- 8 Mbytes flash EEPROM.
  - Note that EEPROM is limited to 10000 write cycles.
- Supports a 64-bit 66/100/133 MHz 3.3 V PCI-X (or a 64-bit 33/66 MHz 3.3 V or 5 V conventional PCI) Host interface.
- Integrated Watchdog circuitry for automatically recovering from application or system failure.
- Supports an external rotary encoder with quadrature output.

Electrical specifications

Matrox Helios XCL	
Operating voltage and current	Typical: 3.3 V, 1.2 A = 3.96 W Typical: 5.0 V, 1.1 A = 5.5 W Typical: 12 V, 0.02 A = 0.24 W Total (typical) = 9.70 W
I/O Specifications	
Input signals in LVDS format	100 Ohm differential termination. Input current: -10 µA (min) to +10 µA (max). Input voltage: • common-mode: 0.1 V (min) to 2.3 V (max). • differential threshold: low of -100 mV (min); high of 100 mV (max).
Output signals in LVDS format	No termination. Output current (loaded 100 Ohm): 3.1 mA (typ). Output voltage (loaded 100 Ohm): • differential: 250 mV (min) to 450 mV (max). • common-mode: 1.125 V (min) to 1.375 V (max). • low: 1.02 V (typ), 0.9 V (min); high: 1.33 V (typ), 1.6 V (max).
Input signals in TTL format	No termination. Pulled up to 3.3 V with 4.7 k ohm. Clamped to -0.7 V and to 5.7 V. Input current: 1 µA (max). Input voltage threshold: low of 0.8 V (max); high of 2.0 V (min).
Output signals in TTL format	22 Ohm series termination. Output current: low of 64 mA (max), high of -32 mA (max). Output voltage: low of 0.55 V (max); high of 3.0 V (min).
Opto-coupled input signals	511 Ohm series termination. Input current: • low: 250 µA (max). • high: 5 mA (min) (6.3 mA recommended) to 15 mA (max) (10 mA recommended). Input voltage (with 511 Ohm series resistor only): low of 0.8 V (max); high of 4.06 V (min) and 9.165 V (max).

Matrox Helios XA	
Operating voltage and current	Typical: 3.3 V, 2 A = 6.6 W Typical: 5.0 V, 1.1 A = 5.5 W Typical: 12 V, 0.42 A = 5.04 W Total (typical) = 17.14 W
Analog data signal specification	75 Ohm termination. Peak signal without saturation: 3 V. Clamped to -5 V and to 5 V (max source current +0.5 A). Amplitude: • 0.25 V (min) to 1.2 V (max) (terminated) if using a maximum gain factor of 4. • 0.5 V (min) to 2.4 V (max) (terminated) if using a maximum gain factor of 2.
I/O Specifications	
Input signals in LVDS format	110 Ohm differential termination. On the analog video input (DVI) connectors: • Input current: -10 µA (min) to +10 µA (max). • Input voltage: - common-mode voltage: 0.1 V (min) to 2.3 V (max). - differential threshold: low of -100 mV (min); high of 100 mV (max). On external auxiliary I/O connector 0: • Differential input current: -1.8 mA (min) to +1.8 mA (max). • Input voltage: - common-mode: -0.5 V (min) to 5 V (max). - differential threshold: low of -200 mV (min); high of 200 mV (max).
Output signals in LVDS format	On the analog video input (DVI) connectors: • No termination. • Output current (loaded 100 Ohm): 3.1 mA (typ). • Output voltage (loaded 100 Ohm): - differential: 250 mV (min) to 450 mV (max). - common-mode: 1.125 V (min) to 1.375 V (max). - low of 1.02 V (typ), 0.9 V (min); high of 1.33 V (typ), 1.6 V (max). On external auxiliary I/O connector 0: • Output current (loaded 100 Ohm): 26 mA total (typ). • Output voltage (loaded 100 Ohm): - differential: 250 mV (min), 450 mV (max). - common-mode: 1.125 V (min), 1.375 V (max).

Matrox Helios XA		
	Input signals in TTL format	On the analog video input (DVI) connectors, for all TTL input signals, except for TTL auxiliary signals that can be configured for trigger input: • No termination. • Clamped to 4 V (max source current +100 mA). • Input current: 5 µA (max). • Input voltage threshold: low of 0.8 V (max); high of 2.0 V (min). On the analog video input (DVI) connectors, only for TTL auxiliary signals that can be configured for trigger input: • No termination. • Pulled up to 5 V with 10 k Ohm. • Clamped to -0.7 V and to 5.7 V. • Input current: 1 µA (max). • Input voltage threshold: low of 0.8 V (max); high of 2.0 V (min). On external auxiliary I/O connector 0: • No termination. • Pulled up to 3.3 V with 4.7 k ohm. • Clamped to -0.7 V. • Input current: 1 µA (max). • Input voltage threshold: low of 0.8 V (max); high of 2.0 V (min).
	Output signals in TTL format	On the analog video input (DVI) connectors, for all TTL output signals, except for TTL auxiliary signals that can be configured for exposure output: • 33 Ohm series impedance. • Output current: low of 24 mA (max), high of -24 mA (max). • Output voltage: low of 0.55 V (max); high of 2.0 V (min). On the analog video input (DVI) connectors, only for TTL auxiliary signals that can be configured for exposure output, and for all TTL output signals on external auxiliary I/O connector 0: • 50 Ohm series impedance. • Output current: low of 64 mA (max), high of -32 mA (max). • Output voltage: low of 0.55 V (max); high of 3.0 V (min).
	Opto-coupled input signals	330 Ohm series termination. Input current: • low: 250 µA (max). • high: 5 mA (min) (6.3 mA recommended) to 15 mA (max) (10 mA recommended). Input voltage (with 330 Ohm series resistor only): low of 0.8 V (max); high of 3.15 V (min) and 6.45 V (max).

Matrox Helios XD		
Operating voltage and current		Typical: 3.3 V, 0.00 A = 0.00 W Typical: 5.0 V, 3.31 A = 18.15 W Typical: 12 V, 0.00 A = 0.00 W Total (typical) = 18.15 W
I/O Specifications		
	Input signals in LVDS format	100 Ohm differential termination. Differential input current: -10 µA (min) to +10 µA (max). Input voltage: • common-mode voltage: 0.1 V (min) to 2.3 V (max). • differential threshold: low of -100 mV (min); high of 100 mV (max).
	Output signals in LVDS/RS-422 format	Output current (loaded 100 Ohm): 26 mA total (typ). Output voltage (loaded 100 Ohm): • differential: 2 V (min), 2.6 V (typ). • common-mode: 2 V (max), 1.5 V (typ).
	Input signals in RS-422 format	100 Ohm differential termination. Differential input current: -1.8 mA (min) to +1.8 mA (max). Input voltage: • common-mode: -0.5 V (min) to 5 V (max). • differential threshold: low of -200 mV (min); high of 200 mV (max).
	Input signals in TTL format	No termination. Pulled up to 3.3 V with 4.7 k ohm. Clamped to -0.7 V and to 5.7 V. Input current: 1 µA (max). Input voltage threshold: low of 0.8 V (max); high of 2.0 V (min).
	Output signals in TTL format	For all TTL/LVDS auxiliary output signals that are configured for TTL output: • No termination. • Output current: low of 64 mA (max), high of -32 mA (max). • Output voltage: low of 0.55 V (max); high of 3.0 V (min). Only for TTL-specific auxiliary output signals: • 22 Ohm series termination. • Output current: low of 64 mA (max), high of -32 mA (max). • Output voltage: low of 0.55 V (max); high of 3.0 V (min).
	Opto-coupled input signals	511 Ohm series termination. Input current: • low: 250 µA (max). • high: 5 mA (min) (6.3 mA recommended) to 15 mA (max) (10 mA recommended). Input voltage (with 511 Ohm series resistor only): low of 0.8 V (max); high of 4.06 V (min) and 9.165 V (max).

Dimensions and environmental specifications

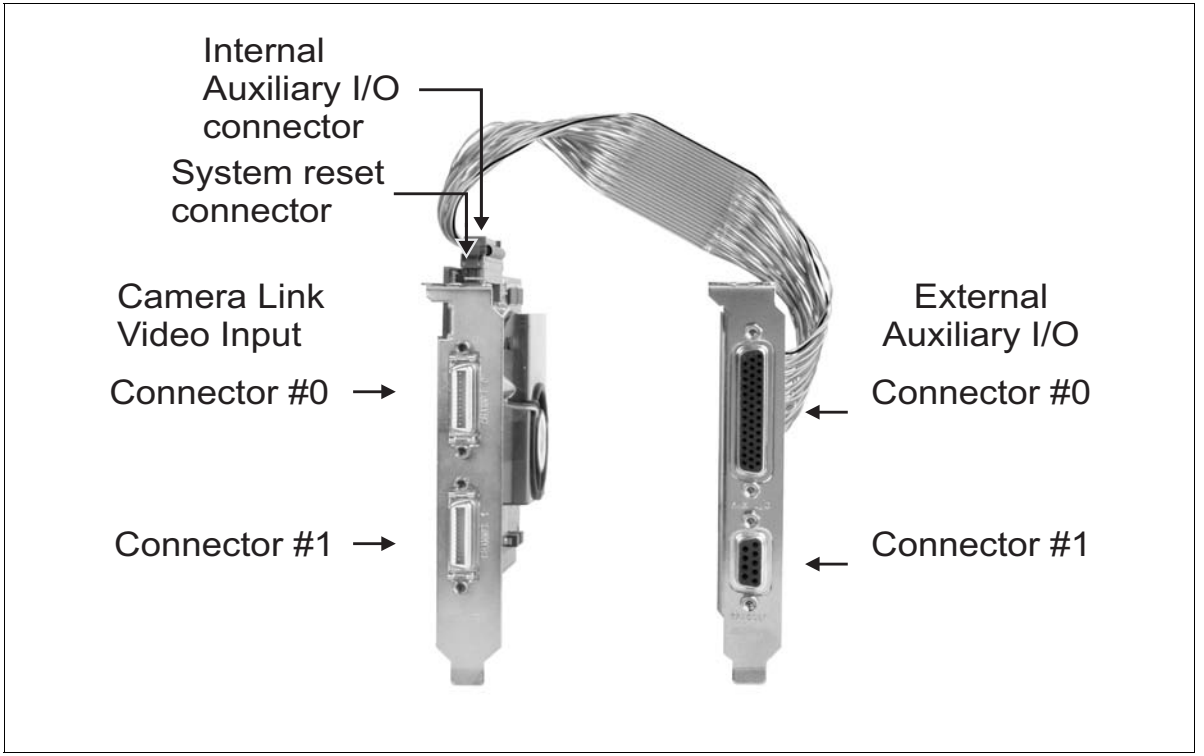
- Matrox Helios XCL:
  - Dimensions: 17.46 L x 10.7 H x 1.73 W cm (6.875" x 4.2" x 0.68") from bottom edge of goldfinger to top edge of board.
  - Ventilation requirements: 50 LFM (linear feet per minute) over board(s).
- Matrox Helios XA and XD:
  - Dimensions: 31.20 L x 10.7 H x 1.73 W cm (12.283" x 4.2" x 0.68") from bottom edge of goldfinger to top edge of board.
  - Ventilation requirements: 50 LFM (linear feet per minute) over board(s).
- Minimum/maximum ambient operating temperature: 0°C to55°C (32°F to 131°F).
- Minimum/maximum storage temperature: -40°C to 75°C.
- Operating humidity: 0 to 95% relative humidity (non-condensing).
- Storage humidity: 0 - 95% relative humidity (non-condensing).
- Maximum altitude of operation: 3000 m
- Maximum altitude of transportation: 12000 m

Connectors on Matrox Helios XCL

The Matrox Helios XCL board has several interface connectors. On its bracket, there are two Camera Link video input connectors. On the top edge of the board, there is an internal auxiliary I/O connector and a system reset connector[1].

On the bracket of the cable adapter board, there are two external auxiliary I/O connectors (HD-44 and DB-9); these allow you to access the signals of the internal auxiliary I/O connector from outside the computer enclosure.

The following illustrates Matrox Helios XCL and an adapter board:

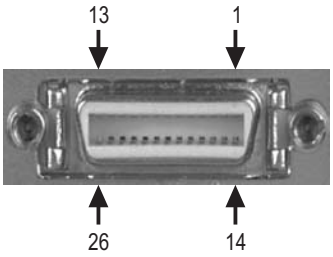


Note that acquisition path is abbreviated as *acq. path* in this section.

1. Starting from revision 1 of the Matrox Helios XCL PCB.

Camera Link video input connectors

The two Camera Link video input connectors are 26-pin high-density mini D ribbon (MDR) connectors. They are used to receive video input, timing, and synchronization signals and transmit/receive communication signals between the video source and the frame grabber. The pinout of these connectors follow the Camera Link standard.



For the dual-Base version, the two Camera Link video input connectors have the same pinout; each connector supports video input from one video source. This pinout is listed in the following table:

Pin	Signal	Description	Pin	Signal	Description
1	Inner shield	Ground.	14	Inner shield	Ground.
2	CC4-	Camera control output 4 (negative). Specific to the acq. path: exposure output 0 or 1; user output 0 or 1.	15	CC4+	Camera control output 4 (positive). Specific to the acq. path: exposure output 0 or 1; user output 0 or 1.
3	CC3+	Camera control output 3 (positive). Specific to the acq. path: exposure output 0 or 1; user output 0 or 1.	16	CC3-	Camera control output 3 (negative). Specific to the acq. path: exposure output 0 or 1; user output 0 or 1.
4	CC2-	Camera control output 2 (negative). Specific to the acq. path: exposure output 0 or 1; user output 0 or 1.	17	CC2+	Camera control output 2 (positive). Specific to the acq. path: exposure output 0 or 1; user output 0 or 1.
5	CC1+	Camera control output 1 (positive). Specific to the acq. path: exposure output 0 or 1; user output 0 or 1.	18	CC1-	Camera control output 1 (negative). Specific to the acq. path: exposure output 0 or 1; user output 0 or 1.
6	SerTFG+	Serial port to frame grabber (UART) (positive).	19	SerTFG-	Serial port to frame grabber (UART) (negative).
7	SerTC-	Serial port to video source (UART) (negative).	20	SerTC+	Serial port to video source (UART) (positive).
8	X3+	Video input data X3 (positive).	21	X3-	Video input data X3 (negative).
9	Xclk+	Clock input X (positive).	22	Xclk-	Clock input X (negative).

Pin	Signal	Description	Pin	Signal	Description
10	X2+	Video input data X2 (positive).	23	X2-	Video input data X2 (negative).
11	X1+	Video input data X1 (positive).	24	X1-	Video input data X1 (negative).
12	X0+	Video input data X0 (positive).	25	X0-	Video input data X0 (negative).
13	Inner shield	Ground.	26	Inner shield	Ground.

For the single-Full version, connector #0 has the same pinout as the one in the previous table. For connector #1, the pinout is listed in the following table. You can only attach one video source to these connectors (or two RGB genlocked video sources); see the *Matrox Helios hardware reference* chapter for more details.

Pin	Signal	Description	Pin	Signal	Description
1	Inner shield	Ground.	14	Inner shield	Ground.
2	Z3+	Video input data Z3 (positive).	15	Z3-	Video input data Z3 (negative).
3	Zclk+	Clock input Z (positive).	16	Zclk-	Clock input Z (negative).
4	Z2+	Video input data Z2 (positive).	17	Z2-	Video input data Z2 (negative).
5	Z1+	Video input data Z1 (positive).	18	Z1-	Video input data Z1 (negative).
6	Z0+	Video input data Z0 (positive).	19	Z0-	Video input data Z0 (negative).
7	TERMINATED	100 Ohm termination between pins 7 and 20.	20	TERMINATED	100 Ohm termination between pins 7 and 20.
8	Y3+	Video input data Y3 (positive).	21	Y3-	Video input data Y3 (negative).
9	Yclk+	Clock input Y (positive).	22	Yclk-	Clock input Y (negative).
10	Y2+	Video input data Y2 (positive).	23	Y2-	Video input data Y2 (negative).
11	Y1+	Video input data Y1 (positive).	24	Y1-	Video input data Y1 (negative).
12	Y0+	Video input data Y0 (positive).	25	Y0-	Video input data Y0 (negative).
13	Inner shield	Ground.	26	Inner shield	Ground.

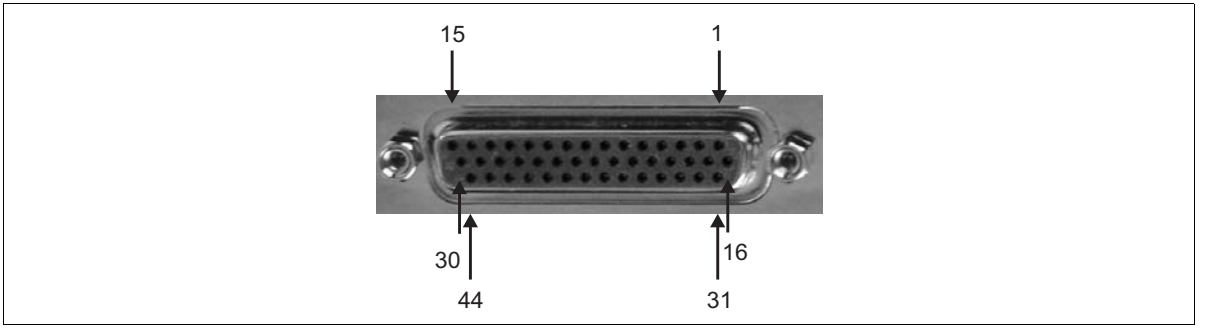
To interface with the above connectors, use a standard Camera Link cable. You can purchase such a cable from your video source manufacturer, 3M Interconnect Solutions for Factory Automation, Intercon 1, or other third parties. Note that this cable is not available from Matrox.

❖ If using both Camera Link connectors on the single-Full version of the board, the cables you choose must be of the same type and length. Otherwise, the cables can have different propagation delays.

External auxiliary I/O connector 0

External auxiliary I/O connector 0 is a high-density DB-44 female connector, located on the bracket of the cable adapter board. It is used to transmit timing and synchronization signals, and transmit/receive auxiliary signals. It interfaces with the 50-pin internal auxiliary I/O connector on the board, making the I/O signals accessible outside the computer enclosure.

The pinout for this connector is as follows. The description of each (positive) auxiliary signal states whether the signal is specific to an independent acquisition path and the type of signals that can be routed onto it.



Pin	Signal	Description
1	P1_TTL_AUX_IO_1	TTL auxiliary input/output 1 for acq. path 1. Supported signals: exposure output 0, trigger input 1, user input/output 3.
2	P1_LVDS_AUX_OUT1+	LVDS auxiliary output 1 for acq. path 1 (positive). Supported signals: exposure output 1, user output 6.
3	P0_LVDS_AUX_OUT1-	LVDS auxiliary output 1 for acq. path 0 (negative). See pin 19 for more information.
4	P0_LVDS_AUX_OUT0-	LVDS auxiliary output 0 for acq. path 0 (negative). See pin 20 for more information.
5	P1_LVDS_HSYNC_OUT-	HSYNC output for acq. path 1 (negative). See pin 6 for more information.
6	P1_LVDS_HSYNC_OUT+	HSYNC output for acq. path 1 (positive).
7	P1_LVDS_CLK_OUT+	Clock output for acq. path 1 (positive).
8	OPTO_AUX_IN0-	Opto-isolated auxiliary input 0 for an unspecified acq. path (negative). See pin 24 for more information.
9	NC	Not connected.
10	NC	Not connected.

Pin	Signal	Description
11	P0_LVDS_CLK_OUT+	Clock output for acq. path 0 (positive).
12	LVDS_AUX_IN1+	LVDS auxiliary input 1 for an unspecified acq. path (positive). Signals only supported for acq. path 0: user input 11. Signals only supported for acq. path 1: trigger input 1, user input 6, timer clock input, or quadrature input bit 1. Signals supported for any acq. path: trigger input 3.
13	P0_TTL_AUX_IO_1	TTL auxiliary input/output 1 for acq. path 0. Supported signals: exposure output 0, trigger input 1, user input/output 3.
14	GND	Ground.
15	TTL_AUX_IO_1	TTL auxiliary input/output 1 for an unspecified acq. path. Signals only supported for acq. path 0: user input/output 7. Signals only supported for acq. path 1: exposure output 1, user input/output 4. Signals supported for any acq. path: trigger input 3.
16	GND	Ground.
17	P1_LVDS_AUX_OUT1-	LVDS auxiliary output 1 for acq. path 1 (negative). See pin 2 for more information.
18	P1_LVDS_AUX_OUT0-	LVDS auxiliary output 0 for acq. path 1 (negative). See pin 33 for more information.
19	P0_LVDS_AUX_OUT1+	LVDS auxiliary output 1 for acq. path 0 (positive). Supported signals: exposure output 1, user output 6.
20	P0_LVDS_AUX_OUT0+	LVDS auxiliary output 0 for acq. path 0 (positive). Supported signals: exposure output 0, user output 5.
21	P1_LVDS_VSYNC_OUT-	VSYNC output for acq. path 1 (negative). See pin 36 for more information.
22	P1_LVDS_CLK_OUT-	Clock output for acq. path 1 (negative). See pin 7 for more information.
23	P0_LVDS_AUX_IN1-	LVDS auxiliary input 1 for acq. path 0 (negative). See pin 37 for more information.
24	OPTO_AUX_IN0+	Opto-isolated auxiliary input 0 for an unspecified acq. path (positive). Signals only supported for acq. path 0: user input 8. Signals only supported for acq. path 1: trigger input 0, user input 0, field polarity input. Signals supported for any acq. path: trigger input 2.
25	P0_LVDS_VSYNC_OUT-	VSYNC output for acq. path 0 (negative). See pin 40 for more information.
26	P0_LVDS_HSYNC_OUT-	HSYNC output for acq. path 0 (negative). See pin 41 for more information.

Pin	Signal	Description
27	P0_LVDS_CLK_OUT-	Clock output for acq. path 0 (negative). See pin 11 for more information.
28	LVDS_AUX_IN1-	LVDS auxiliary input 1 for an unspecified acq. path (negative). See pin 12 for more information.
29	GND	Ground.
30	GND	Ground.
31	LVDS_AUX_IN0-	LVDS auxiliary input 0 for an unspecified acq. path (negative). See pin 32 for more information.
32	LVDS_AUX_IN0+	LVDS auxiliary input 0 for an unspecified acq. path (positive). Signals only supported for acq. path 0: user input 10. Signals only supported for acq. path 1: trigger input 0, user input 5, field polarity input, or quadrature input bit 0. Signals supported for any acq.acq. path: trigger input 2.
33	P1_LVDS_AUX_OUT0+	LVDS auxiliary output 0 for acq. path 1 (positive). Supported signals: exposure output 0, user output 5.
34	GND	Ground.
35	P1_TTL_AUX_IO_0	TTL auxiliary input/output 0 for acq. path 1. Supported signals: trigger input 0, user input/output 2, field input.
36	P1_LVDS_VSYNC_OUT+	VSYNC output for acq. path 1 (positive).
37	P0_LVDS_AUX_IN1+	LVDS auxiliary input 1 for acq. path 0 (positive). Supported signals: trigger input 1, user input 6, timer clock input, or quadrature input bit 1.
38	OPTO_AUX_IN1+	Opto-isolated auxiliary input 1 for an unspecified acq. path (positive). Signals only supported for acq. path 0: user input 9. Signals only supported for acq. path 1: trigger input 1, user input 1. Signals supported for any acq. path: trigger input 3.
39	OPTO_AUX_IN1-	Opto-isolated auxiliary input 1 for an unspecified acq. path (negative). See pin 38 for more information.
40	P0_LVDS_VSYNC_OUT+	VSYNC output for acq. path 0 (positive).
41	P0_LVDS_HSYNC_OUT+	HSYNC output for acq. path 0 (positive).
42	GND	Ground.
43	TTL_AUX_IO_0	TTL auxiliary input/output 0 for an unspecified acq. path. Signals only supported for acq. path 0: exposure output 1, user input/output 4. Signals only supported for acq. path 1: user input/output 7. Signals supported for any acq. path: trigger input 2.
44	NC	Not connected.

To build your own cable, you can purchase the following parts:

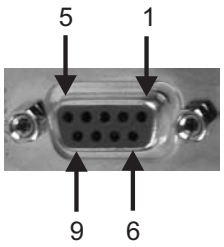
Manufacturer:	NorComp, Inc.
Connector:	180-044-102-001
Backshell:	970-025-010-011

These parts can be purchased from third parties such as Digi-Key Corporation (www.digikey.com).

External auxiliary I/O connector 1

External auxiliary I/O connector 1 is a standard DB-9 female connector, located on the bracket of the cable adapter board. It is used to transmit/receive auxiliary signals. It interfaces with the 50-pin internal auxiliary I/O connector on the board, making the I/O signals accessible outside the computer enclosure.

The pinout for this connector is as follows. The description of each (positive) auxiliary signal states whether the signal is specific to an independent acquisition path and the type of signals that can be routed onto it.



Pin	Signal	Description
1	P0_TTL_AUX_IO_0	TTL auxiliary input/output 0 for acq. path 0. Supported signals: trigger input 0, user input/output 2, field input.
2	P0_OPTO_AUX_IN0-	Opto-isolated auxiliary input 0 for acq. path 0 (negative). See pin 7 for more information.
3	P0_LVDS_AUX_IN0-	LVDS auxiliary input 0 for acq. path 0 (negative). See pin 8 for more information.
4	P0_OPTO_AUX_IN1+	Opto-isolated auxiliary input 1 for acq. path 0 (positive). Supported signals: trigger input 1, user input 1.
5	P0_OPTO_AUX_IN1-	Opto-isolated auxiliary input 1 for acq. path 0 (negative). See pin 4 for more information.

Pin	Signal	Description
6	GND	Ground.
7	P0_OPTO_AUX_IN0+	Opto-isolated auxiliary input 0 for acq. path 0 (positive). Supported signals: trigger input 0, user input 0, field input.
8	P0_LVDS_AUX_IN0+	LVDS auxiliary input 0 for acq. path 0 (positive). Supported signals: trigger input 0, user input 5, field input, or quadrature input bit 0.
9	NC	Not connected.

To build your own cable, you can purchase the following parts:

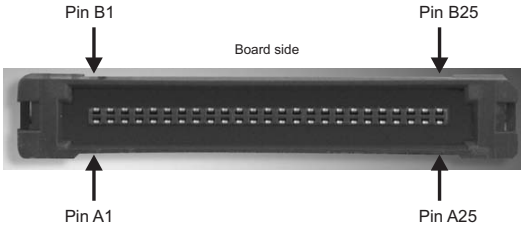
Manufacturer:	NorComp, Inc.
Connector:	172-E09-102-031
Backshell:	970-009-010-011

These parts can be purchased from third parties such as Digi-Key Corporation (www.digikey.com).

Internal auxiliary I/O connector

The internal auxiliary I/O connector is a 50-pin low-profile IDC connector. It is used to transmit timing and synchronization signals, and transmit/receive auxiliary signals. The connector is located on the edge of the board, making the signals accessible from inside the computer enclosure.

The pinout for this connector is as follows. Refer to the description of the external auxiliary I/O connectors to establish if an auxiliary signal is specific to an independent acquisition path and the type of signals that can be routed onto it.

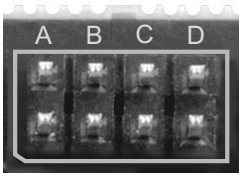


Pin	Signal	Description	Pin	Signal	Description
A1	P0_LVDS_HSYNC_OUT+	HSYNC output for acq. path 0 (positive).	B1	P0_LVDS_HSYNC_OUT-	HSYNC output for acq. path 0 (negative).
A2	GND	Ground.	B2	P1_LVDS_HSYNC_OUT-	HSYNC output for acq. path 1 (negative).
A3	P1_LVDS_HSYNC_OUT+	HSYNC output for acq. path 1 (positive).	B3	GND	Ground.
A4	P0_LVDS_VSYNC_OUT+	VSYNC output for acq. path 0 (positive).	B4	P0_LVDS_VSYNC_OUT-	VSYNC output for acq. path 0 (negative).
A5	P1_LVDS_VSYNC_OUT+	VSYNC output for acq. path 1 (positive).	B5	P1_LVDS_VSYNC_OUT-	VSYNC output for acq. path 1 (negative).
A6	P0_TTL_AUX_IO_0	TTL auxiliary input/output 0 for acq. path 0.	B6	TTL_AUX_IO_0	TTL auxiliary input/output 0 for an unspecified acq. path.
A7	P0_TTL_AUX_IO_1	TTL auxiliary input/output 1 for acq. path 0.	B7	GND	Ground.
A8	P1_TTL_AUX_IO_0	TTL auxiliary input/output 0 for acq. path 1.	B8	P1_TTL_AUX_IO_1	TTL auxiliary input/output 1 for acq. path 1.
A9	GND	Ground.	B9	P0_LVDS_AUX_IN0-	LVDS auxiliary input 0 for acq. path 0 (negative).
A10	P0_LVDS_AUX_IN0+	LVDS auxiliary input 0 for acq. path 0 (positive).	B10	P0_LVDS_AUX_IN1-	LVDS auxiliary input 1 for acq. path 0 (negative).
A11	P0_LVDS_AUX_IN1+	LVDS auxiliary input 1 for acq. path 0 (positive).	B11	LVDS_AUX_IN0-	LVDS auxiliary input 0 for an unspecified acq. path (negative).
A12	LVDS_AUX_IN0+	LVDS auxiliary input 0 for an unspecified acq. path (positive).	B12	GND	Ground.
A13	LVDS_AUX_IN1+	LVDS auxiliary input 1 for an unspecified acq. path (positive).	B13	LVDS_AUX_IN1-	LVDS auxiliary input 1 for an unspecified acq. path (negative).
A14	P0_LVDS_AUX_OUT0+	LVDS auxiliary output 0 for acq. path 0 (positive).	B14	P0_LVDS_AUX_OUT0-	LVDS auxiliary output 0 for acq. path 0 (negative).
A15	P0_LVDS_AUX_OUT1+	LVDS auxiliary output 1 for acq. path 0 (positive).	B15	P0_LVDS_AUX_OUT1-	LVDS auxiliary output 1 for acq. path 0 (negative).
A16	P1_LVDS_AUX_OUT0+	LVDS auxiliary output 0 for acq. path 1 (positive).	B16	P1_LVDS_AUX_OUT0-	LVDS auxiliary output 0 for acq. path 1 (negative).
A17	P1_LVDS_AUX_OUT1+	LVDS auxiliary output 1 for acq. path 1 (positive).	B17	P1_LVDS_AUX_OUT1-	LVDS auxiliary output 1 for acq. path 1 (negative).
A18	TTL_AUX_IO_1	TTL auxiliary input/output 1 for an unspecified acq. path.	B18	GND	Ground.
A19	P0_LVDS_CLK_OUT+	Clock output for acq. path 0 (positive).	B19	P0_LVDS_CLK_OUT-	Clock output for acq. path 0 (negative).

Pin	Signal	Description	Pin	Signal	Description
A20	GND	Ground.	B20	P1_LVDS_CLK_OUT-	Clock output for acq. path 1 (negative).
A21	P1_LVDS_CLK_OUT+	Clock output for acq. path 1 (positive).	B21	GND	Ground.
A22	P0_OPTO_AUX_IN0-	Opto-isolated auxiliary input 0 for acq. path 0 (negative).	B22	P0_OPTO_AUX_IN0+	Opto-isolated auxiliary input 0 for acq. path 0 (positive).
A23	P0_OPTO_AUX_IN1-	Opto-isolated auxiliary input 1 for acq. path 0 (negative).	B23	P0_OPTO_AUX_IN1+	Opto-isolated auxiliary input 1 for acq. path 0 (positive).
A24	OPTO_AUX_IN0-	Opto-isolated auxiliary input 0 for an unspecified acq. path (negative).	B24	OPTO_AUX_IN0+	Opto-isolated auxiliary input 0 for an unspecified acq. path (positive).
A25	OPTO_AUX_IN1-	Opto-isolated auxiliary input 1 for an unspecified acq. path (negative).	B25	OPTO_AUX_IN1+	Opto-isolated auxiliary input 1 for an unspecified acq. path (positive).

System reset connector

The system reset connector is standard, 0.1" spacing, 8-pin male connector, used to reset the motherboard if the reset button is pressed or the Watchdog circuitry of Matrox Helios detects abnormal Host inactivity. The system reset connector's pin assignment is as follows. Note that pin 1 is denoted with the triangular etching in the image.



Matrox Helios XCL

Pin pair	Pin	Signal	Description
A	1	RESET_MB	Reset signal output (usually to motherboard).
	2	GND_MB	Motherboard active reset level (usually ground).
B	1	RESET_BUTTON	Reset signal input (usually from Reset button).
	2	GND_MB	Motherboard active reset level (usually ground).
C	1 and 2		Reserved.
D	1 and 2		Reserved.

To build your own cable, parts can be purchased from:

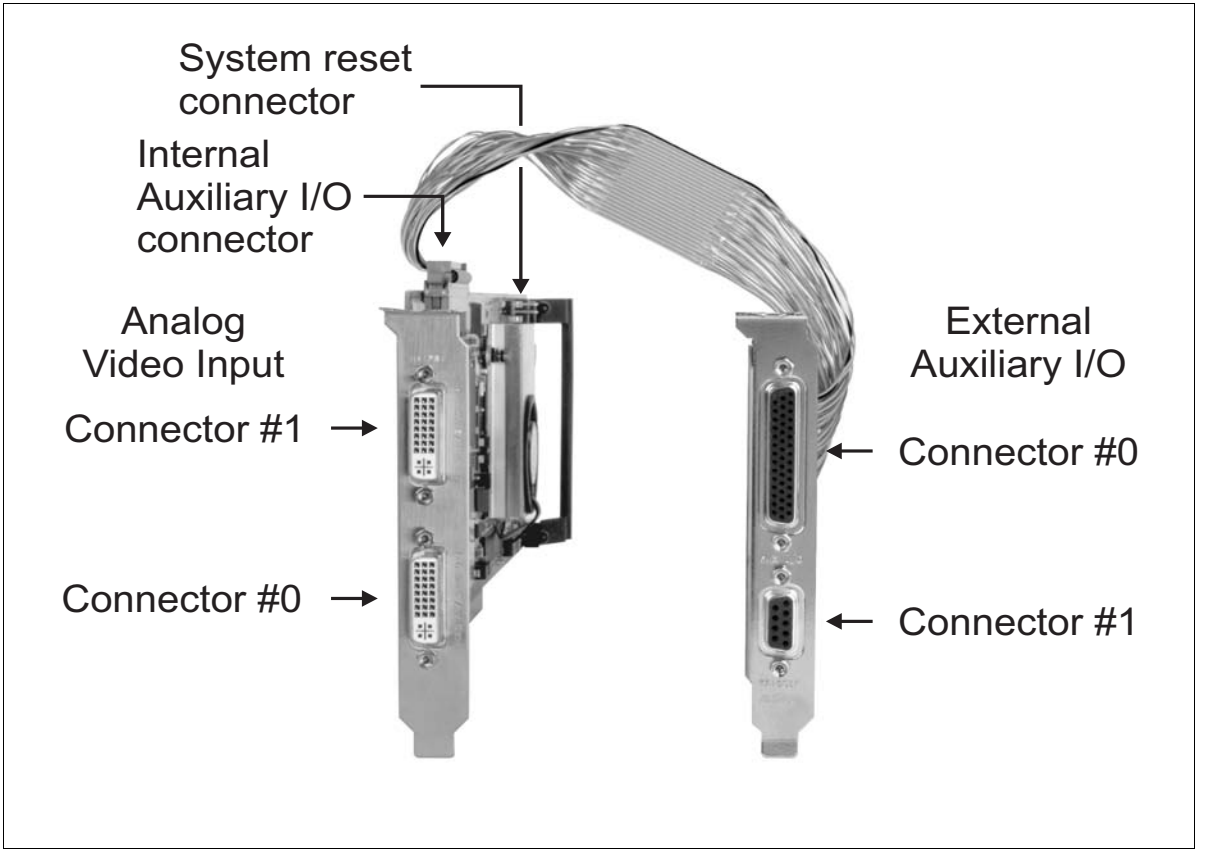
Manufacturer	FCI
Crimp-to-wire receptacle	76357-301 (discrete contact; wire size: 22-30 AWG)
Housing	65039-035 (2 positions)

Connectors on Matrox Helios XA

The Matrox Helios XA has several interface connectors. On its bracket, there are two analog video input connectors (DVI type). On the top edge of the board, there is an internal auxiliary I/O connector and a system reset connector.

On the bracket of the cable adapter board, there are two external auxiliary I/O connectors (HD-44 and DB-9); these allow you to access the signals of the internal auxiliary I/O connector from outside the computer enclosure.

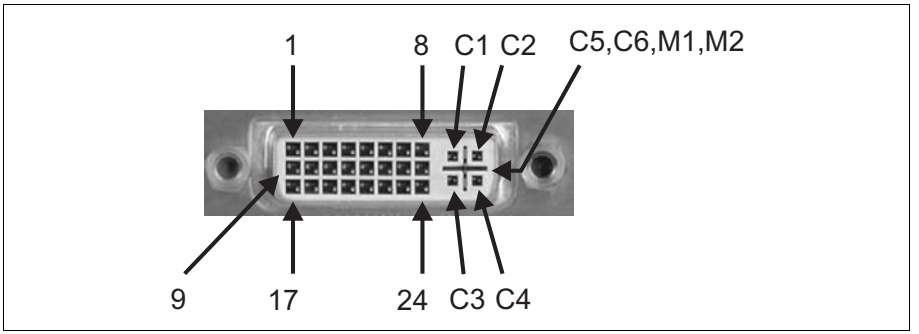
The following illustrates Matrox Helios XA and an adapter board:



Note that acquisition path is abbreviated as *acq. path* in this section.

Analog video input connectors

The two analog video input connectors are DVI dual-video-input female connectors. They are used to receive video input signals and transmit/receive timing, synchronization, and communication signals between the video source and the frame grabber.



Important

To connect the output of a display board (with a DVI output connector) to the analog video input connectors, you can use a standard cable (DVI-I to DVI-I or DVI-A to DVI-A cable) if the display board encodes the synchronization signals on the video data (sync on green). Otherwise, you must use the Matrox DVI-TO-8BNC/O cable or a custom cable that re-routes the synchronization signals to the appropriate pins.

Note that synchronization and clock signals can be either LVDS or TTL; when TTL, they are expected on the pin denoted as positive.

The pinout for DVI connector 0 is as follows:

Pin	Signal	Description	Pin	Signal	Description
1	P1_LVDS/TTL_VSYNC_IO-	VSYNC input/output for acq. path 1 (negative).	17	P1_LVDS/TTL_CLK_IO-	Clock input/output for acq. path 1 (negative).
2	P1_LVDS/TTL_VSYNC_IO+	VSYNC input/output for acq. path 1 (positive).	18	P1_LVDS/TTL_CLK_IO+	Clock input/output for acq. path 1 (positive).
3	GND	Ground.	19	GND	Ground.
4	P0_LVDS/TTL_VSYNC_IO-	VSYNC input/output for acq. path 0 (negative).	20	P0_LVDS/TTL_CLK_IO-	Clock input/output for acq. path 0 (negative).
5	P0_LVDS/TTL_VSYNC_IO+	VSYNC input/output for acq. path 0 (positive).	21	P0_LVDS/TTL_CLK_IO+	Clock input/output for acq. path 0 (positive).

Pin	Signal	Description	Pin	Signal	Description
6	P1_TTL_AUX(EXP)_OUT	TTL auxiliary output for acq. path 1. Supported signals: exposure output 0 (main purpose) or user output 2.	22	P1_TTL_AUX(TRIG)_IN	TTL auxiliary input for acq. path 1. Supported signals: trigger input 0 (main purpose), field input, or user input 0.
7	P1_RS232_RxD	RS-232 serial port 1 to frame grabber (UART).	23	P0_TTL_AUX(EXP)_OUT	TTL auxiliary output for acq. path 0. Supported signals: exposure output 0 (main purpose) or user output 2 .
8	P1_RS232_TxD	RS-232 serial port 1 to video source (UART).	24	P0_RS232_RxD	RS-232 serial port 0 to frame grabber (UART).
9	P1_LVDS/TTL_CHSYNC_IO-	CSYNC input or HSYNC input/output for acq. path 1 (negative).	C1	P0_VID_IN_A	Video input A for acq. path 0 (AC/DC).
10	P1_LVDS/TTL_CHSYNC_IO+	CSYNC input or HSYNC input/output for acq. path 1 (positive).	C2	P1_VID_IN_A	Video input A for acq. path 1 (AC/DC).
11	GND	Ground.	C3	P2_VID_IN_A	Video input A for acq. path 2 (AC/DC).
12	P0_LVDS/TTL_CHSYNC_IO-	CSYNC input or HSYNC input/output for acq. path 0 (negative).	C4	P3_VID_IN_A	Video input A for acq. path 3 (AC/DC).
13	P0_LVDS/TTL_CHSYNC_IO+	CSYNC input or HSYNC input/output for acq. path 0 (positive).	C5	GND	Ground.
14	P0_TTL_AUX(TRIG)_IN	TTL auxiliary input for acq. path 0. Supported signals: trigger input 0 (main purpose) , field input, or user input 0.	C6	GND	Ground.
15	GND	Ground.	M1	GND	Ground.
16	P0_RS232_TxD	RS-232 serial port 0 to video source (UART).	M2	GND	Ground.

The pinout for DVI connector 1 is as follows:

Pin	Signal	Description	Pin	Signal	Description
1	P3_LVDS/TTL_VSYNC_IO-	VSYNC input/output for acq. path 3 (negative).	17	P3_LVDS/TTL_CLK_IO-	Clock input/output for acq. path 3 (negative).
2	P3_LVDS/TTL_VSYNC_IO+	VSYNC input/output for acq. path 3 (positive).	18	P3_LVDS/TTL_CLK_IO+	Clock input/output for acq. path 3 (positive).
3	GND	Ground.	19	GND	Ground.

Pin	Signal	Description	Pin	Signal	Description
4	P2_LVDS/TTL_VSYNC_IO-	VSYNC input/output for acq. path 2 (negative).	20	P2_LVDS/TTL_CLK_IO-	Clock input/output for acq. path 2 (negative).
5	P2_LVDS/TTL_VSYNC_IO+	VSYNC input/output for acq. path 2 (positive).	21	P2_LVDS/TTL_CLK_IO+	Clock input/output for acq. path 2 (positive).
6	P3_TTL_AUX(EXP)_OUT	TTL auxiliary output for acq. path 3. Supported signals: exposure output 0 (main purpose) or user output 2.	22	P3_TTL_AUX(TRIG)_IN	TTL auxiliary input for acq. path 3. Supported signals: trigger input 0 (main purpose), field input, or user input 0.
7	P3_RS232_RxD	RS-232 serial port 3 to frame grabber (UART).	23	P2_TTL_AUX(EXP)_OUT	TTL auxiliary output for acq. path 2. Supported signals: exposure output 0 (main purpose) or user output 2.
8	P3_RS232_TxD	RS-232 serial port 3 to video source (UART).	24	P2_RS232_RxD	RS-232 serial port 2 to frame grabber (UART).
9	P3_LVDS/TTL_CHSYNC_IO-	CSYNC input or HSYNC input/output for acq. path 3 (negative).	C1	P0_VID_IN_B	Video input B for acq. path 0 (AC/DC).
10	P3_LVDS/TTL_CHSYNC_IO+	CSYNC input or HSYNC input/output for acq. path 3 (positive).	C2	P1_VID_IN_B	Video input B for acq. path 1 (AC/DC).
11	GND	Ground.	C3	P2_VID_IN_B	Video input B for acq. path 2 (AC/DC).
12	P2_LVDS/TTL_CHSYNC_IO-	CSYNC input or HSYNC input/output for acq. path 2 (negative).	C4	P3_VID_IN_B	Video input B for acq. path 3 (AC/DC).
13	P2_LVDS/TTL_CHSYNC_IO+	CSYNC input or HSYNC input/output for acq. path 2 (positive).	C5	GND	Ground.
14	P2_TTL_AUX(TRIG)_IN	TTL auxiliary input for acq. path 2. Supported signals: trigger input 0 (main purpose), field input, or user input 0.	C6	GND	Ground.
15	GND	Ground.	M1	GND	Ground.
16	P2_RS232_TxD	RS-232 serial port 2 to video source (UART).	M2	GND	Ground.

To build your own cable, parts can be purchased from:

Manufacturer:	JAE Electronics
Connector:	DV2P029M11

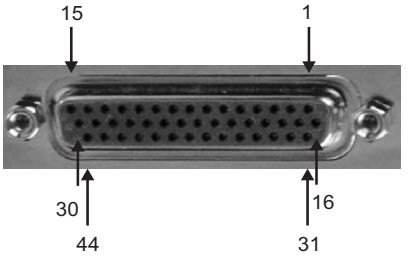
External auxiliary I/O connector 0

External auxiliary I/O connector 0 is a high-density DB-44 female connector, located on the bracket of the LVDS cable adapter board. This connector interfaces with the 50-pin internal auxiliary I/O connector on the board. This connector is used to transmit/receive auxiliary signals; these signals can be used to route synchronization, trigger, exposure, or user-defined signals.

The pins for auxiliary signals carry unidirectional signals, unlike those for synchronization signals on the DVI connector. This means that using this connector, the board can both transmit and receive synchronization signals at the same time.

In addition, all the signals can be either LVDS or TTL; when TTL, they are expected on the pin denoted as positive.

The pinout for this connector is as follows. The description of each (positive) auxiliary signal states whether the signal is specific to an independent acquisition path and the type of signals that can be routed onto it.



Pin	Signal	Description
1	LVDS/TTL_AUX_IN7+	Auxiliary input 7 for an unspecified acq. path (positive). Signals only supported for acq. path 0, 1, and 2: user input 9. Signals only supported for acq. path 3: user input 3, timer clock, VSYNC input, or quadrature input bit 1. Signals supported for any acq. path: trigger input 3.
2	P3_LVDS/TTL_AUX_OUT1+	Auxiliary output 1 for acq. path 3 (positive). Supported signals: user output 1, exposure output 1, or VSYNC output.
3	GND	Ground.
4	P2_LVDS/TTL_AUX_OUT1-	Auxiliary output 1 for acq. path 2 (negative). See pin 20 for more information.

Pin	Signal	Description
5	LVDS/TTL_AUX_IN5-	Auxiliary input 5 for an unspecified acq. path (negative). See pin 6 for more information.
6	LVDS/TTL_AUX_IN5+	Auxiliary input 5 for an unspecified acq. path (positive). Signals only supported for acq. path 0 and 1: user input 7. Signals only supported for acq. path 2: user input 3, timer clock, VSYNC input, or quadrature input bit 1. Signals only supported for acq. path 3: user input 9. Signals supported for any acq. path: trigger input 3.
7	LVDS/TTL_AUX_IN4+	Auxiliary input 4 for an unspecified acq. path (positive). Signals only supported for acq. path 0 and 1: user input 6. Signals only supported for acq. path 2: user input 2, field, data valid, CSYNC, HSYNC input, or quadrature input bit 0. Signals only supported for acq. path 3: user input 8. Signals supported for any acq. path: trigger input 2.
8	LVDS/TTL_AUX_IN2+	Auxiliary input 2 for an unspecified acq. path (positive). Signals only supported for acq. path 0: user input 4. Signals only supported for acq. path 1: user input 2, field, data valid, CSYNC, HSYNC input, or quadrature input bit 0. Signals only supported for acq. path 2 and 3: user input 6. Signals supported for any acq. path: trigger input 2.
9	GND	Ground.
10	GND	Ground.
11	P1_LVDS/TTL_AUX_OUT1+	Auxiliary output 1 for acq. path 1 (positive). Supported signals: user output 1, exposure output 1, or VSYNC output.
12	LVDS/TTL_AUX_IN1+	Auxiliary input 1 for an unspecified acq. path (positive). Signals only supported for acq. path 0: user input 3, timer clock, VSYNC input, or quadrature input bit 1. Signals only supported for acq. path 1, 2, and 3: user input 5. Signals supported for any acq. path: trigger input 3.
13	GND	Ground.
14	GND	Ground.
15	P0_LVDS/TTL_AUX_OUT0+	Auxiliary output 0 for acq. path 0 (positive). Supported signals: user output 0, exposure output 0, or HSYNC output.
16	LVDS/TTL_AUX_IN7-	Auxiliary input 7 for an unspecified acq. path (negative). See pin 1 for more information.
17	P3_LVDS/TTL_AUX_OUT1-	Auxiliary output 1 for acq. path 3 (negative). See pin 2 for more information.

Pin	Signal	Description
18	P3_LVDS/TTL_AUX_OUT0-	Auxiliary output 0 for acq. path 3 (negative). See pin 33 for more information.
19	GND	Ground.
20	P2_LVDS/TTL_AUX_OUT1+	Auxiliary output 1 for acq. path 2 (positive). Supported signals: user output 1, exposure output 1, or VSYNC output.
21	GND	Ground.
22	LVDS/TTL_AUX_IN4-	Auxiliary input 4 for an unspecified acq. path (negative). See pin 7 for more information.
23	GND	Ground.
24	LVDS/TTL_AUX_IN2-	Auxiliary input 2 for an unspecified acq. path (negative). See pin 8 for more information.
25	P2_LVDS/TTL_AUX_OUT0-	Auxiliary output 0 for acq. path 2 (negative). See pin 40 for more information.
26	GND	Ground.
27	P1_LVDS/TTL_AUX_OUT1-	Auxiliary output 1 for acq. path 1 (negative). See pin 11 for more information.
28	LVDS/TTL_AUX_IN1-	Auxiliary input 1 for an unspecified acq. path (negative). See pin 12 for more information.
29	P0_LVDS/TTL_AUX_OUT1-	Auxiliary output 1 for acq. path 0 (negative). See pin 44 for more information.
30	P0_LVDS/TTL_AUX_OUT0-	Auxiliary output 0 for acq. path 0 (negative). See pin 15 for more information.
31	LVDS/TTL_AUX_IN6-	Auxiliary input 6 for an unspecified acq. path (negative). See pin 32 for more information.
32	LVDS/TTL_AUX_IN6+	Auxiliary input 6 for an unspecified acq. path (positive). Signals only supported for acq. path 0, 1, and 2: user input 8. Signals only supported for acq. path 3: user input 2, field, data valid, CSYNC, HSYNC input, or quadrature input bit 0. Signals supported for any acq. path: trigger input 2.
33	P3_LVDS/TTL_AUX_OUT0+	Auxiliary output 0 for acq. path 3 (positive). Supported signals: user output 0, exposure output 0, or HSYNC output.
34	LVDS/TTL_AUX_IN0-	Auxiliary input 0 for an unspecified acq. path (negative). See pin 35 for more information.

Pin	Signal	Description
35	LVDS/TTL_AUX_IN0+	Auxiliary input 0 for an unspecified acq. path (positive). Signals only supported for acq. path 0: user input 2, field, data valid, CSYNC, HSYNC input, or quadrature input bit 0. Signals only supported for acq. path 1, 2, and 3: user input 4. Signals supported for any acq. path: trigger input 2.
36	GND	Ground.
37	GND	Ground.
38	LVDS/TTL_AUX_IN3-	Auxiliary input 3 for an unspecified acq. path (negative). See pin 39 for more information.
39	LVDS/TTL_AUX_IN3+	Auxiliary input 3 for an unspecified acq. path (positive). Signals only supported for acq. path 0: user input 5. Signals only supported for acq. path 1: user input 3, timer clock, VSYNC input, or quadrature input bit 1. Signals only supported for acq. path 2 and 3: user input 7. Signals supported for any acq. path: trigger input 3.
40	P2_LVDS/TTL_AUX_OUT0+	Auxiliary output 0 for acq. path 2 (positive). Supported signals: user output 0, exposure output 0, or HSYNC output.
41	GND	Ground.
42	P1_LVDS/TTL_AUX_OUT0-	Auxiliary output 0 for acq. path 1 (negative). See pin 43 for more information.
43	P1_LVDS/TTL_AUX_OUT0+	Auxiliary output 0 for acq. path 1 (positive). Supported signals: user output 0, exposure output 0, or HSYNC output.
44	P0_LVDS/TTL_AUX_OUT1+	Auxiliary output 1 for acq. path 0 (positive). Supported signals: user output 1, exposure output 1, or VSYNC output.

To build your own cable, you can purchase the following parts:

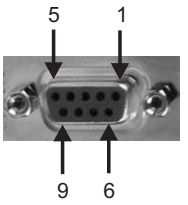
Manufacturer:	NorComp, Inc.
Connector:	180-044-102-001
Backshell:	970-025-010-011

These parts can be purchased from third parties such as Digi-Key Corporation (www.digikey.com).

External auxiliary I/O connector 1

External auxiliary I/O connector 1 is a standard DB-9 female connector, located on the bracket of the LVDS cable adapter board. It is used to receive opto-isolated auxiliary input signals. It interfaces with the 50-pin internal auxiliary I/O connector on the board, making the auxiliary signals accessible outside the computer enclosure.

The pinout for this connector is as follows.The description of each (positive) auxiliary signal states whether the signal is specific to an independent acquisition path and the type of signals that can be routed onto it. .



Pin	Signal	Description
1	P2_OPTO_AUX(TRIG)_IN+	Opto-isolated auxiliary input for acq. path 2 (positive). Supported signals: trigger input 1 or user input 1.
2	P0_OPTO_AUX(TRIG)_IN-	Opto-isolated auxiliary input for acq. path 0 (negative). See pin 7 for more information.
3	P3_OPTO_AUX(TRIG)_IN-	Opto-isolated auxiliary input for acq. path 3 (negative). See pin 8 for more information.
4	P1_OPTO_AUX(TRIG)_IN+	Opto-isolated auxiliary input for acq. path 1 (positive). Supported signals: trigger input 1 or user input 1.
5	P1_OPTO_AUX(TRIG)_IN-	Opto-isolated auxiliary input for acq. path 1 (negative). See pin 4 for more information.
6	P2_OPTO_AUX(TRIG)_IN-	Opto-isolated auxiliary input for acq. path 2 (negative). See pin 1 for more information.
7	P0_OPTO_AUX(TRIG)_IN+	Opto-isolated auxiliary input for acq. path 0 (positive). Supported signals: trigger input 1 or user input 1.
8	P3_OPTO_AUX(TRIG)_IN+	Opto-isolated auxiliary input for acq. path 3 (positive). Supported signals: trigger input 1 or user input 1.
9	NC	Not connected.

To build your own cable, you can purchase the following parts:

Manufacturer:	NorComp, Inc.
Connector:	172-E09-102-031
Backshell:	970-009-010-011

These parts can be purchased from third parties such as Digi-Key Corporation (www.digikey.com).

Internal auxiliary I/O connector

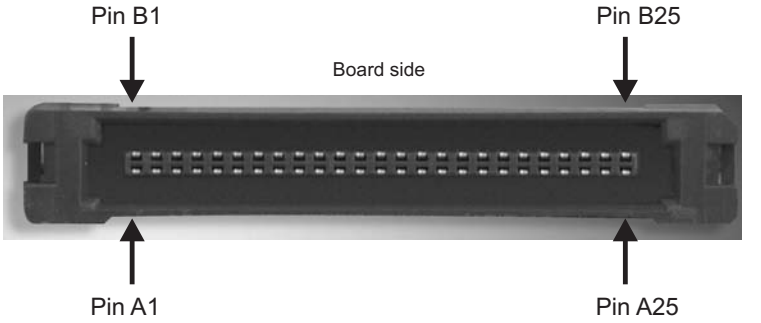
The internal auxiliary I/O connector is a 50-pin low-profile IDC connector. lt is used to transmit/receive the camera control, timing, and auxiliary signals. The auxiliary signals can be used to route synchronization, trigger, exposure, or user-defined signals.

The connector is located on the edge of the board, making the signals accessible from inside the computer enclosure. You can use the connectors on the adapter board to access most of these signals from outside the computer enclosure; only the most commonly used signals are accessible so that an easily sourced connector of a reasonable size can be used. Note that the clock signals are not accessible from the adapter board.

The pins for auxiliary signals carry unidirectional signals, unlike those for synchronization signals on the DVI connector. This means that using this connector, the board can both transmit and receive synchronization signals at the same time.

All the signals are LVTTL signals unless otherwise specified. Note that the clock and synchronization signals are the LVTTL version of those on the DVI connectors.

The pinout for this connector is as follows. Refer to the description of the external auxiliary I/O connectors to establish if an auxiliary signal is specific to an independent acquisition path and the type of signals that can be routed onto it..

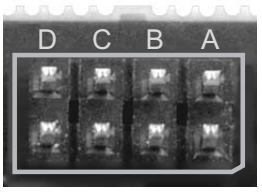


Pin	Signal	Description	Pin	Signal	Description
A1	5 V	5 V power.	B1	5 V	5 V power.
A2	GND	Ground.	B2	P0_LVTTL_CLK_OUT	Clock output for acq. path 0.
A3	GND	Ground.	B3	P0_LVTTL_CLK_IN	Clock input for acq. path 0.
A4	GND	Ground.	B4	P1_LVTTL_CLK_OUT	Clock output for acq. path 1.
A5	GND	Ground.	B5	P1_LVTTL_CLK_IN	Clock input for acq. path 1.
A6	GND	Ground.	B6	P2_LVTTL_CLK_OUT	Clock output for acq. path 2.
A7	GND	Ground.	B7	P2_LVTTL_CLK_IN	Clock input for acq. path 2.
A8	GND	Ground.	B8	P3_LVTTL_CLK_OUT	Clock output for acq. path 3.
A9	GND	Ground.	B9	P3_LVTTL_CLK_IN	Clock input for acq. path 3.
A10	P0_LVTTL_AUX(TRIG)_IN	Auxiliary input 0 for acq. path 0 (main purpose: trigger 1) from external auxiliary I/O connector 1.	B10	P1_LVTTL_AUX(TRIG)_IN	Auxiliary input 1 for acq. path 1 (main purpose: trigger 1) from external auxiliary I/O connector 1.
A11	P2_LVTTL_AUX(TRIG)_IN	Auxiliary input 2 for acq. path 2 (main purpose: trigger 1) from external auxiliary I/O connector 1.	B11	P3_LVTTL_AUX(TRIG)_IN	Auxiliary input 3 for acq. path 3 (main purpose: trigger 1) from external auxiliary I/O connector 1.
A12	P0_LVTTL_AUX_OUT0	Auxiliary output 0 for acq. path 0.	B12	P0_LVTTL_AUX_OUT1	Auxiliary output 1 for acq. path 0.
A13	P1_LVTTL_AUX_OUT0	Auxiliary output 0 for acq. path 1.	B13	P1_LVTTL_AUX_OUT1	Auxiliary output 1 for acq. path 1.
A14	P2_LVTTL_AUX_OUT0	Auxiliary output 0 for acq. path 2.	B14	P2_LVTTL_AUX_OUT1	Auxiliary output 1 for acq. path 2.
A15	P3_LVTTL_AUX_OUT0	Auxiliary output 0 for acq. path 3.	B15	P3_LVTTL_AUX_OUT1	Auxiliary output 1 for acq. path 3.
A16	P0_CTRL_AUX_OUT	LVDS/TTL selector for acq. path 0.	B16	P1_CTRL_AUX_OUT	LVDS/TTL selector for acq. path 1.

Pin	Signal	Description	Pin	Signal	Description
A17	P2_CTRL_AUX_OUT	LVDS/TTL selector for acq. path 2.	B17	P3_CTRL_AUX_OUT	LVDS/TTL selector for acq. path 3.
A18	3.3 V	3.3 V power .	B18	3.3 V	3.3 V power.
A19	GND	Ground.	B19	GND	Ground.
A20	LVTTL_AUX_IN0	Auxiliary input 0 for an unspecified acq. path.	B20	LVTTL_AUX_IN1	Auxiliary input 1 for an unspecified acq. path.
A21	LVTTL_AUX_IN2	Auxiliary input 2 for an unspecified acq. path.	B21	LVTTL_AUX_IN3	Auxiliary input 3 for an unspecified acq. path.
A22	LVTTL_AUX_IN4	Auxiliary input 4 for an unspecified acq. path.	B22	LVTTL_AUX_IN5	Auxiliary input 5 for an unspecified acq. path.
A23	LVTTL_AUX_IN6	Auxiliary input 6 for an unspecified acq. path.	B23	LVTTL_AUX_IN7	Auxiliary input 7 for an unspecified acq. path.
A24	CTRL_AUX_IN0-1	LVDS/TTL selector. for auxiliary input 0 and 1.	B24	CTRL_AUX_IN2-3	LVDS/TTL selector for auxiliary input 2 and 3.
A25	CTRL_AUX_IN4-5	LVDS/TTL selector for auxiliary input 4 and 5.	B25	CTRL_AUX_IN6-7	LVDS/TTL selector for auxiliary input 6 and 7.

System reset connector

The system reset connector is a standard, 0.1" spacing, 8-pin male connector, used to reset the motherboard if the reset button is pressed or the Watchdog circuitry of Matrox Helios detects abnormal Host inactivity. The system reset connector's pin assignment is as follows. Note that pin 1 is denoted with the triangular etching in the image.



Matrox Helios XA

Pin pair	Pin	Signal	Description
A	1	RESET_MB	Reset signal output (usually to motherboard).
	2	GND_MB	Motherboard active reset level (usually ground).
B	1	RESET_BUTTON	Reset signal input (usually from Reset button).
	2	GND_MB	Motherboard active reset level (usually ground).

Pin pair	Pin	Signal	Description
C	1 and 2	-	Reserved.
D	1 and 2	-	Reserved.

To build your own cable, parts can be purchased from:

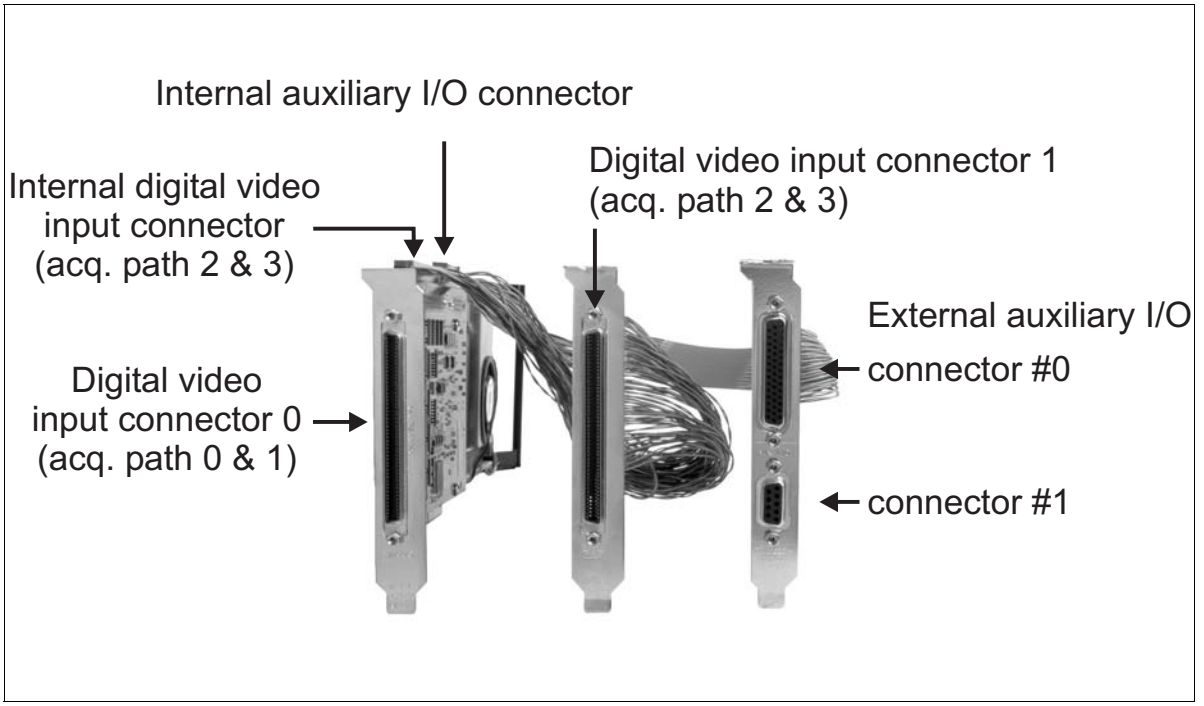
Manufacturer	FCI
Crimp-to-wire receptacle	76357-301 (discrete contact; wire size: 22-30 AWG)
Housing	65039-035 (2 positions)

Connectors on Matrox Helios XD

Matrox Helios XD has several interface connectors. On its bracket, there is a digital video input connector (for acquisition paths 0 and 1). On its top edge, there is an internal digital video input connector (for acquisition paths 2 and 3), an internal auxiliary I/O connector, and a system reset connector.

On the bracket of one of the cable adapter boards, there is digital video input connector to access the signals of the internal digital video input connector from outside the computer enclosure. On the bracket of the other cable adapter board, there are two external auxiliary I/O connectors (HD-44 and DB-9); these allow you to access the signals of the internal auxiliary I/O connector from outside the computer enclosure.

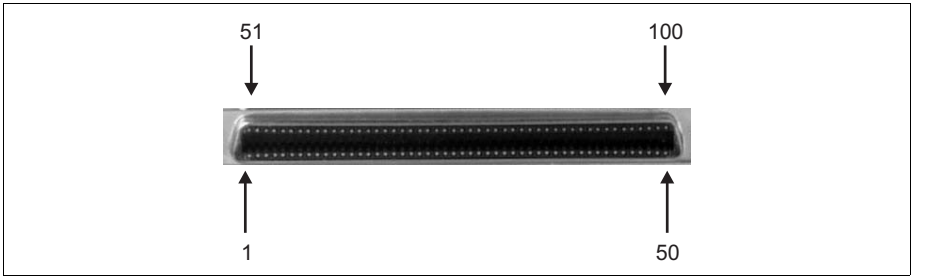
The following illustrates Matrox Helios XD with the two cable adapter boards:



Note that acquisition path is abbreviated as *acq. path* in this section.

Digital video input connectors

The two digital connectors are 100-pin low-profile IDC female connectors (recepticals). They are used to receive video input signals and transmit/receive timing, synchronization, and communication signals between the video source and the frame grabber.



Connector 0 has the following pinout:

Pin	Signal	Description
1	P0_LVDS_DATA_IN0+	Data bit 0 for acq. path 0, in LVDS format (positive).
2	P0_LVDS_DATA_IN0-	Data bit 0 for acq. path 0, in LVDS format (negative).
3	P0_LVDS_DATA_IN1+	Data bit 1 for acq. path 0, in LVDS format (positive).
4	P0_LVDS_DATA_IN1-	Data bit 1 for acq. path 0, in LVDS format (negative).
5	P0_LVDS_DATA_IN2+	Data bit 2 for acq. path 0, in LVDS format (positive).
6	P0_LVDS_DATA_IN2-	Data bit 2 for acq. path 0, in LVDS format (negative).
7	P0_LVDS_DATA_IN3+	Data bit 3 for acq. path 0, in LVDS format (positive).
8	P0_LVDS_DATA_IN3-	Data bit 3 for acq. path 0, in LVDS format (negative).
9	P0_LVDS_DATA_IN4+	Data bit 4 for acq. path 0, in LVDS format (positive).
10	P0_LVDS_DATA_IN4-	Data bit 4 for acq. path 0, in LVDS format (negative).
11	P0_LVDS_DATA_IN5+	Data bit 5 for acq. path 0, in LVDS format (positive).
12	P0_LVDS_DATA_IN5-	Data bit 5 for acq. path 0, in LVDS format (negative).
13	P0_LVDS_DATA_IN6+	Data bit 6 for acq. path 0, in LVDS format (positive).
14	P0_LVDS_DATA_IN6-	Data bit 6 for acq. path 0, in LVDS format (negative).
15	P0_LVDS_DATA_IN7+	Data bit 7 for acq. path 0, in LVDS format (positive).
16	P0_LVDS_DATA_IN7-	Data bit 7 for acq. path 0, in LVDS format (negative).
17	P0_LVDS_DATA_IN8+	Data bit 8 for acq. path 0, in LVDS format (positive).
18	P0_LVDS_DATA_IN8-	Data bit 8 for acq. path 0, in LVDS format (negative).
19	P0_LVDS_DATA_IN9+	Data bit 9 for acq. path 0, in LVDS format (positive).

Pin	Signal	Description
20	P0_LVDS_DATA_IN9-	Data bit 9 for acq. path 0, in LVDS format (negative).
21	P0_LVDS_DATA_IN10+	Data bit 10 for acq. path 0, in LVDS format (positive).
22	P0_LVDS_DATA_IN10-	Data bit 10 for acq. path 0, in LVDS format (negative).
23	P0_LVDS_DATA_IN11+	Data bit 11 for acq. path 0, in LVDS format (positive).
24	P0_LVDS_DATA_IN11-	Data bit 11 for acq. path 0, in LVDS format (negative).
25	P0_LVDS_DATA_IN12+	Data bit 12 for acq. path 0, in LVDS format (positive).
26	P0_LVDS_DATA_IN12-	Data bit 12 for acq. path 0, in LVDS format (negative).
27	P0_LVDS_DATA_IN13+	Data bit 13 for acq. path 0, in LVDS format (positive).
28	P0_LVDS_DATA_IN13-	Data bit 13 for acq. path 0, in LVDS format (negative).
29	P0_LVDS_DATA_IN14+	Data bit 14 for acq. path 0, in LVDS format (positive).
30	P0_LVDS_DATA_IN14-	Data bit 14 for acq. path 0, in LVDS format (negative).
31	P0_LVDS_DATA_IN15+	Data bit 15 for acq. path 0, in LVDS format (positive).
32	P0_LVDS_DATA_IN15-	Data bit 15 for acq. path 0, in LVDS format (negative).
33	P0_LVDS_HSYNC_IN+	HSYNC input for acq. path 0, in LVDS format (positive).
34	P0_LVDS_HSYNC_IN-	HSYNC input for acq. path 0, in LVDS format (negative).
35	P0_LVDS_AUX(VSYNC)_IN+	LVDS auxiliary input for acq. path 0 (positive). Supported signals: user input 0, trigger input 0, or VSYNC input (main purpose).
36	P0_LVDS_AUX(VSYNC)_IN-	LVDS auxiliary input for acq. path 0 (negative). See pin 35 for more information.
37	P0_LVDS_AUX(CLK)_OUT+	LVDS auxiliary output for acq. path 0 (positive). Supported signals: user output 0 or clock output (main purpose).
38	P0_LVDS_AUX(CLK)_OUT-	LVDS auxiliary output for acq. path 0 (negative). See pin 37 for more information.
39	P0_LVDS_CLK_IN+	Clock input for acq. path 0, in LVDS format (positive).
40	P0_LVDS_CLK_IN-	Clock input for acq. path 0, in LVDS format (negative).
41	P0_LVDS/TTL_AUX(HSYNC)_OUT0+	LVDS/TTL auxiliary output 0 for acq. path 0 (positive). Supported signals: HSYNC output (main purpose) or user output 1.
42	P0_LVDS/TTL_AUX(HSYNC)_OUT0-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary output 0 for acq. path 0. See pin 41 for more information.
43	P0_LVDS/TTL_AUX(VSYNC)_OUT1+	LVDS/TTL auxiliary output 1 for acq. path 0 (positive). Supported signals: VSYNC output (main purpose) or user output 2.
44	P0_LVDS/TTL_AUX(VSYNC)_OUT1-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary output 1 for acq. path 0. See pin 43 for more information.
45	P0_LVDS/TTL_AUX(EXP)_OUT2+	LVDS/TTL auxiliary output 2 for acq. path 0 (positive). Supported signals: exposure output 0 (main purpose) or user output 3.

Pin	Signal	Description
46	P0_LVDS/TTL_AUX(EXP)_OUT2-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary output 2 for acq. path 0. See pin 45 for more information.
47	P0_LVDS/TTL_AUX(EXP)_OUT3+	LVDS/TTL auxiliary output 3 for acq. path 0 (positive). Supported signals: exposure output 1 (main purpose) or user output 4.
48	P0_LVDS/TTL_AUX(EXP)_OUT3-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary output 3 for acq. path 0. See pin 47 for more information.
49	P0_TTL_AUX(TRIG)_IO	TTL auxiliary input/output for acq. path 0. Supported signals: trigger input 1 (main purpose), user input 3, or user output 5.
50	GND	Ground
51	P1_LVDS_DATA_IN0+	Data bit 0 for acq. path 1, in LVDS format (positive).
52	P1_LVDS_DATA_IN0-	Data bit 0 for acq. path 1, in LVDS format (negative).
53	P1_LVDS_DATA_IN1+	Data bit 1 for acq. path 1, in LVDS format (positive).
54	P1_LVDS_DATA_IN1-	Data bit 1 for acq. path 1, in LVDS format (negative).
55	P1_LVDS_DATA_IN2+	Data bit 2 for acq. path 1, in LVDS format (positive).
56	P1_LVDS_DATA_IN2-	Data bit 2 for acq. path 1, in LVDS format (negative).
57	P1_LVDS_DATA_IN3+	Data bit 3 for acq. path 1, in LVDS format (positive).
58	P1_LVDS_DATA_IN3-	Data bit 3 for acq. path 1, in LVDS format (negative).
59	P1_LVDS_DATA_IN4+	Data bit 4 for acq. path 1, in LVDS format (positive).
60	P1_LVDS_DATA_IN4-	Data bit 4 for acq. path 1, in LVDS format (negative).
61	P1_LVDS_DATA_IN5+	Data bit 5 for acq. path 1, in LVDS format (positive).
62	P1_LVDS_DATA_IN5-	Data bit 5 for acq. path 1, in LVDS format (negative).
63	P1_LVDS_DATA_IN6+	Data bit 6 for acq. path 1, in LVDS format (positive).
64	P1_LVDS_DATA_IN6-	Data bit 6 for acq. path 1, in LVDS format (negative).
65	P1_LVDS_DATA_IN7+	Data bit 7 for acq. path 1, in LVDS format (positive).
66	P1_LVDS_DATA_IN7-	Data bit 7 for acq. path 1, in LVDS format (negative).
67	P1_LVDS_DATA_IN8+	Data bit 8 for acq. path 1, in LVDS format (positive).
68	P1_LVDS_DATA_IN8-	Data bit 8 for acq. path 1, in LVDS format (negative).
69	P1_LVDS_DATA_IN9+	Data bit 9 for acq. path 1, in LVDS format (positive).
70	P1_LVDS_DATA_IN9-	Data bit 9 for acq. path 1, in LVDS format (negative).
71	P1_LVDS_DATA_IN10+	Data bit 10 for acq. path 1, in LVDS format (positive).
72	P1_LVDS_DATA_IN10-	Data bit 10 for acq. path 1, in LVDS format (negative).
73	P1_LVDS_DATA_IN11+	Data bit 11 for acq. path 1, in LVDS format (positive).
74	P1_LVDS_DATA_IN11-	Data bit 11 for acq. path 1, in LVDS format (negative).
75	P1_LVDS_DATA_IN12+	Data bit 12 for acq. path 1, in LVDS format (positive).

Pin	Signal	Description
76	P1_LVDS_DATA_IN12-	Data bit 12 for acq. path 1, in LVDS format (negative).
77	P1_LVDS_DATA_IN13+	Data bit 13 for acq. path 1, in LVDS format (positive).
78	P1_LVDS_DATA_IN13-	Data bit 13 for acq. path 1, in LVDS format (negative).
79	P1_LVDS_DATA_IN14+	Data bit 14 for acq. path 1, in LVDS format (positive).
80	P1_LVDS_DATA_IN14-	Data bit 14 for acq. path 1, in LVDS format (negative).
81	P1_LVDS_DATA_IN15+	Data bit 15 for acq. path 1, in LVDS format (positive).
82	P1_LVDS_DATA_IN15-	Data bit 15 for acq. path 1, in LVDS format (negative).
83	P1_LVDS_HSYNC_IN+	HSYNC input for acq. path 1, in LVDS format (positive).
84	P1_LVDS_HSYNC_IN-	HSYNC input for acq. path 1, in LVDS format (negative).
85	P1_LVDS_AUX(VSYNC)_IN+	LVDS auxiliary input for acq. path 1 (positive). Supported signals: user input 0, trigger input 0, or VSYNC input (main purpose).
86	P1_LVDS_AUX(VSYNC)_IN-	LVDS auxiliary input for acq. path 1 (negative). See pin 85 for more information.
87	P1_LVDS_AUX(CLK)_OUT+	LVDS auxiliary output for acq. path 1 (positive). Supported signals: user output 0 or clock output (main purpose).
88	P1_LVDS_AUX(CLK)_OUT-	LVDS auxiliary output for acq. path 1 (negative). See pin 87 for more information.
89	P1_LVDS_CLK_IN+	Clock input for acq. path 1, in LVDS format (positive).
90	P1_LVDS_CLK_IN-	Clock input for acq. path 1, in LVDS format (negative).
91	P1_LVDS/TTL_AUX(HSYNC)_OUT0+	LVDS/TTL auxiliary output 0 for acq. path 1 (positive). Supported signals: HSYNC output (main purpose) or user output 1.
92	P1_LVDS/TTL_AUX(HSYNC)_OUT0-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary output 0 for acq. path 1. See pin 91 for more information.
93	P1_LVDS/TTL_AUX(VSYNC)_OUT1+	LVDS/TTL auxiliary output 1 for acq. path 1 (positive). Supported signals: VSYNC output (main purpose) or user output 2.
94	P1_LVDS/TTL_AUX(VSYNC)_OUT1-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary output 1 for acq. path 1. See pin 93 for more information.
95	P1_LVDS/TTL_AUX(EXP)_OUT2+	LVDS/TTL auxiliary output 2 for acq. path 1 (positive). Supported signals: exposure output 0 (main purpose) or user output 3.
96	P1_LVDS/TTL_AUX(EXP)_OUT2-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary output 2 for acq. path 1. See pin 95 for more information.
97	P1_LVDS/TTL_AUX(EXP)_OUT3+	LVDS/TTL auxiliary output 3 for acq. path 1 (positive). Supported signals: exposure output 1 (main purpose) or user output 4.
98	P1_LVDS/TTL_AUX(EXP)_OUT3-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary output 3 for acq. path 1. See pin 97 for more information.

Pin	Signal	Description
99	P1_TTL_AUX(TRIG)_IO	TTL auxiliary input/output for acq. path 1. Supported signals: trigger input 1 (main purpose), user input 3, or user output 5.
100	GND	Ground

Connector 1 has the following pinout:

Pin	Signal	Description
1	P2_LVDS_DATA_IN0+	Data bit 0 for acq. path 2, in LVDS format (positive).
2	P2_LVDS_DATA_IN0-	Data bit 0 for acq. path 2, in LVDS format (negative).
3	P2_LVDS_DATA_IN1+	Data bit 1 for acq. path 2, in LVDS format (positive).
4	P2_LVDS_DATA_IN1-	Data bit 1 for acq. path 2, in LVDS format (negative).
5	P2_LVDS_DATA_IN2+	Data bit 2 for acq. path 2, in LVDS format (positive).
6	P2_LVDS_DATA_IN2-	Data bit 2 for acq. path 2, in LVDS format (negative).
7	P2_LVDS_DATA_IN3+	Data bit 3 for acq. path 2, in LVDS format (positive).
8	P2_LVDS_DATA_IN3-	Data bit 3 for acq. path 2, in LVDS format (negative).
9	P2_LVDS_DATA_IN4+	Data bit 4 for acq. path 2, in LVDS format (positive).
10	P2_LVDS_DATA_IN4-	Data bit 4 for acq. path 2, in LVDS format (negative).
11	P2_LVDS_DATA_IN5+	Data bit 5 for acq. path 2, in LVDS format (positive).
12	P2_LVDS_DATA_IN5-	Data bit 5 for acq. path 2, in LVDS format (negative).
13	P2_LVDS_DATA_IN6+	Data bit 6 for acq. path 2, in LVDS format (positive).
14	P2_LVDS_DATA_IN6-	Data bit 6 for acq. path 2, in LVDS format (negative).
15	P2_LVDS_DATA_IN7+	Data bit 7 for acq. path 2, in LVDS format (positive).
16	P2_LVDS_DATA_IN7-	Data bit 7 for acq. path 2, in LVDS format (negative).
17	P2_LVDS_DATA_IN8+	Data bit 8 for acq. path 2, in LVDS format (positive).
18	P2_LVDS_DATA_IN8-	Data bit 8 for acq. path 2, in LVDS format (negative).
19	P2_LVDS_DATA_IN9+	Data bit 9 for acq. path 2, in LVDS format (positive).
20	P2_LVDS_DATA_IN9-	Data bit 9 for acq. path 2, in LVDS format (negative).
21	P2_LVDS_DATA_IN10+	Data bit 10 for acq. path 2, in LVDS format (positive).
22	P2_LVDS_DATA_IN10-	Data bit 10 for acq. path 2, in LVDS format (negative).
23	P2_LVDS_DATA_IN11+	Data bit 11 for acq. path 2, in LVDS format (positive).
24	P2_LVDS_DATA_IN11-	Data bit 11 for acq. path 2, in LVDS format (negative).
25	P2_LVDS_DATA_IN12+	Data bit 12 for acq. path 2, in LVDS format (positive).
26	P2_LVDS_DATA_IN12-	Data bit 12 for acq. path 2, in LVDS format (negative).
27	P2_LVDS_DATA_IN13+	Data bit 13 for acq. path 2, in LVDS format (positive).

Pin	Signal	Description
28	P2_LVDS_DATA_IN13-	Data bit 13 for acq. path 2, in LVDS format (negative).
29	P2_LVDS_DATA_IN14+	Data bit 14 for acq. path 2, in LVDS format (positive).
30	P2_LVDS_DATA_IN14-	Data bit 14 for acq. path 2, in LVDS format (negative).
31	P2_LVDS_DATA_IN15+	Data bit 15 for acq. path 2, in LVDS format (positive).
32	P2_LVDS_DATA_IN15-	Data bit 15 for acq. path 2, in LVDS format (negative).
33	P2_LVDS_HSYNC_IN+	HSYNC input for acq. path 2, in LVDS format (positive).
34	P2_LVDS_HSYNC_IN-	HSYNC input for acq. path 2, in LVDS format (negative).
35	P2_LVDS_AUX(VSYNC)_IN+	LVDS auxiliary input for acq. path 2 (positive). Supported signals: user input 0, trigger input 0, or VSYNC input (main purpose).
36	P2_LVDS_AUX(VSYNC)_IN-	LVDS auxiliary input for acq. path 2 (negative). See pin 35 for more information.
37	P2_LVDS_AUX(CLK)_OUT+	LVDS auxiliary output for acq. path 2 (positive). Supported signals: user output 0 or clock output (main purpose).
38	P2_LVDS_AUX(CLK)_OUT-	LVDS auxiliary output for acq. path 2 (negative). See pin 37 for more information.
39	P2_LVDS_CLK_IN+	Clock input for acq. path 2, in LVDS format (positive).
40	P2_LVDS_CLK_IN-	Clock input for acq. path 2, in LVDS format (negative).
41	P2_LVDS/TTL_AUX(HSYNC)_OUT0+	LVDS/TTL auxiliary output 0 for acq. path 2 (positive). Supported signals: HSYNC output (main purpose) or user output 1.
42	P2_LVDS/TTL_AUX(HSYNC)_OUT0-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary output 0 for acq. path 2. See pin 41 for more information.
43	P2_LVDS/TTL_AUX(VSYNC)_OUT1+	LVDS/TTL auxiliary output 1 for acq. path 2 (positive). Supported signals: VSYNC output (main purpose) or user output 2.
44	P2_LVDS/TTL_AUX(VSYNC)_OUT1-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary output 1 for acq. path 2. See pin 43 for more information.
45	P2_LVDS/TTL_AUX(EXP)_OUT2+	LVDS/TTL auxiliary output 2 for acq. path 2 (positive). Supported signals: exposure output 0 (main purpose) or user output 3.
46	P2_LVDS/TTL_AUX(EXP)_OUT2-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary output 2 for acq. path 2 format. See pin 45 for more information.
47	P2_LVDS/TTL_AUX(EXP)_OUT3+	LVDS/TTL auxiliary output 3 for acq. path 2 (positive). Supported signals: exposure output 1 (main purpose) or user output 4.
48	P2_LVDS/TTL_AUX(EXP)_OUT3-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary output 3 for acq. path 2. See pin 47 for more information.
49	P2_TTL_AUX(TRIG)_IO	TTL auxiliary input/output for acq. path 2. Supported signals: trigger input 1 (main purpose), user input 3, or user output 5.

Pin	Signal	Description
50	GND	Ground
51	P3_LVDS_DATA_IN0+	Data bit 0 for acq. path 3, in LVDS format (positive).
52	P3_LVDS_DATA_IN0-	Data bit 0 for acq. path 3, in LVDS format (negative).
53	P3_LVDS_DATA_IN1+	Data bit 1 for acq. path 3, in LVDS format (positive).
54	P3_LVDS_DATA_IN1-	Data bit 1 for acq. path 3, in LVDS format (negative).
55	P3_LVDS_DATA_IN2+	Data bit 2 for acq. path 3, in LVDS format (positive).
56	P3_LVDS_DATA_IN2-	Data bit 2 for acq. path 3, in LVDS format (negative).
57	P3_LVDS_DATA_IN3+	Data bit 3 for acq. path 3, in LVDS format (positive).
58	P3_LVDS_DATA_IN3-	Data bit 3 for acq. path 3, in LVDS format (negative).
59	P3_LVDS_DATA_IN4+	Data bit 4 for acq. path 3, in LVDS format (positive).
60	P3_LVDS_DATA_IN4-	Data bit 4 for acq. path 3, in LVDS format (negative).
61	P3_LVDS_DATA_IN5+	Data bit 5 for acq. path 3, in LVDS format (positive).
62	P3_LVDS_DATA_IN5-	Data bit 5 for acq. path 3, in LVDS format (negative).
63	P3_LVDS_DATA_IN6+	Data bit 6 for acq. path 3, in LVDS format (positive).
64	P3_LVDS_DATA_IN6-	Data bit 6 for acq. path 3, in LVDS format (negative).
65	P3_LVDS_DATA_IN7+	Data bit 7 for acq. path 3, in LVDS format (positive).
66	P3_LVDS_DATA_IN7-	Data bit 7 for acq. path 3, in LVDS format (negative).
67	P3_LVDS_DATA_IN8+	Data bit 8 for acq. path 3, in LVDS format (positive).
68	P3_LVDS_DATA_IN8-	Data bit 8 for acq. path 3, in LVDS format (negative).
69	P3_LVDS_DATA_IN9+	Data bit 9 for acq. path 3, in LVDS format (positive).
70	P3_LVDS_DATA_IN9-	Data bit 9 for acq. path 3, in LVDS format (negative).
71	P3_LVDS_DATA_IN10+	Data bit 10 for acq. path 3, in LVDS format (positive).
72	P3_LVDS_DATA_IN10-	Data bit 10 for acq. path 3, in LVDS format (negative).
73	P3_LVDS_DATA_IN11+	Data bit 11 for acq. path 3, in LVDS format (positive).
74	P3_LVDS_DATA_IN11-	Data bit 11 for acq. path 3, in LVDS format (negative).
75	P3_LVDS_DATA_IN12+	Data bit 12 for acq. path 3, in LVDS format (positive).
76	P3_LVDS_DATA_IN12-	Data bit 12 for acq. path 3, in LVDS format (negative).
77	P3_LVDS_DATA_IN13+	Data bit 13 for acq. path 3, in LVDS format (positive).
78	P3_LVDS_DATA_IN13-	Data bit 13 for acq. path 3, in LVDS format (negative).
79	P3_LVDS_DATA_IN14+	Data bit 14 for acq. path 3, in LVDS format (positive).
80	P3_LVDS_DATA_IN14-	Data bit 14 for acq. path 3, in LVDS format (negative).
81	P3_LVDS_DATA_IN15+	Data bit 15 for acq. path 3, in LVDS format (positive).
82	P3_LVDS_DATA_IN15-	Data bit 15 for acq. path 3, in LVDS format (negative).
83	P3_LVDS_HSYNC_IN+	HSYNC input for acq. path 3, in LVDS format (positive).

Pin	Signal	Description
84	P3_LVDS_HSYNC_IN-	HSYNC input for acq. path 3, in LVDS format (negative).
85	P3_LVDS_AUX(VSYNC)_IN+	LVDS auxiliary input for acq. path 3 (positive). Supported signals: user input 0, trigger input 0, or VSYNC input (main purpose).
86	P3_LVDS_AUX(VSYNC)_IN-	LVDS auxiliary input for acq. path 3 (negative). See pin 85 for more information.
87	P3_LVDS_AUX(CLK)_OUT+	LVDS auxiliary output for acq. path 3 (positive). Supported signals: user output 0 or clock output (main purpose).
88	P3_LVDS_AUX(CLK)_OUT-	LVDS auxiliary output for acq. path 3 (negative). See pin 87 for more information.
89	P3_LVDS_CLK_IN+	Clock input for acq. path 3, in LVDS format (positive).
90	P3_LVDS_CLK_IN-	Clock input for acq. path 3, in LVDS format (negative).
91	P3_LVDS/TTL_AUX(HSYNC)_OUT0+	LVDS/TTL auxiliary output 0 for acq. path 3 (positive). Supported signals: HSYNC output (main purpose) or user output 1.
92	P3_LVDS/TTL_AUX(HSYNC)_OUT0-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary output 0 for acq. path 3. See pin 91 for more information.
93	P3_LVDS/TTL_AUX(VSYNC)_OUT1+	LVDS/TTL auxiliary output 1 for acq. path 3 (positive). Supported signals: VSYNC output (main purpose) or user output 2.
94	P3_LVDS/TTL_AUX(VSYNC)_OUT1-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary output 1 for acq. path 3. See pin 93 for more information.
95	P3_LVDS/TTL_AUX(EXP)_OUT2+	LVDS/TTL auxiliary output 2 for acq. path 3 (positive). Supported signals: exposure output 0 (main purpose) or user output 3.
96	P3_LVDS/TTL_AUX(EXP)_OUT2-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary output 2 for acq. path 3. See pin 95 for more information.
97	P3_LVDS/TTL_AUX(EXP)_OUT3+	LVDS/TTL auxiliary output 3 for acq. path 3 (positive). Supported signals: exposure output 1 (main purpose) or user output 4.
98	P3_LVDS/TTL_AUX(EXP)_OUT3-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary output 3 for acq. path 3. See pin 97 for more information.
99	P3_TTL_AUX(TRIG)_IO	TTL auxiliary input/output for acq. path 3. Supported signals: trigger input 1 (main purpose), user input 3, or user output 5.
100	GND	Ground

You can use the open-ended Matrox DBHD100-TO-OPEN cable to interface with this connector. This cable has a 100-pin low-profile IDC connector at one end, and open-ended wires at the other end.

If building your own cable, you can purchase the following part:

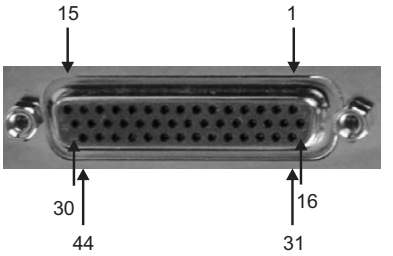
Manufacturer:	ACON Advanced-Connectek Inc.
Connector and shell:	HBP50-1AK3202

Ensure that the cable is a twisted-pair type cable, twisted along signal pairs.

External auxiliary I/O connector 0

External auxiliary I/O connector 0 is a high-density DB-44 female connector, located on the bracket of the cable adapter board. This connector is used to transmit/receive communication and auxiliary signals; the auxiliary signals can be used to route data valid, field, timer clock, trigger, exposure, or user-defined signals. This connector interfaces with the 50-pin internal auxiliary I/O connector on the board, making the I/O signals accessible outside of the computer enclosure.

The pinout for this connector is as follows. The description of each (positive) auxiliary signal states whether the signal is specific to an acquisition path and the type of signals that can be routed onto it.



Pin	Signal	Description
1	P0_RS232_RxD	RS-232 serial input to acq. path 0 of frame grabber (UART).
2	P0_OPTO_AUX(TRIG)_IN0+	Opto-isolated auxiliary input for acq. path 0 (positive). Supported signals: trigger input 0 (main purpose) or user input 4.
3	GND	Ground
4	LVDS/TTL_AUX(TRIG)_IN0-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary input 0 for an unspecified acq. path (negative). See pin 20 for more information.
5	LVDS/TTL_AUX(TRIG)_IN1-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary input 1 for an unspecified acq. path (negative). See pin 6 for more information.

Pin	Signal	Description
6	LVDS/TTL_AUX(TRIG)_IN1+	LVDS/TTL auxiliary input 1 for an unspecified acq. path (positive). Signals only supported for acq. path 0: field polarity input, timer clock input, user input 2, or quadrature input bit 1. Signlas only supported for acq. path 1, 2, and 3: user input 7. Signals supported for any acq. path: trigger input 3 (main purpose).
7	LVDS/TTL_AUX(TRIG)_IN2+	LVDS/TTL auxiliary input 2 for an unspecified acq. path (positive). Signals only supported for acq. path 0: user input 6. Signals only supported for acq. path 1: data valid input and user input 1, or quadrature input bit 0. Signals only supported for acq. path_2 and 3: user input 8. Signals supported for any acq. path: trigger input 2 (main purpose).
8	P0_TTL_AUX(EXP)_OUT	TTL auxiliary output for acq. path 0. Supported signals: exposure output 0 (main purpose) or user output 6.
9	GND	Ground
10	GND	Ground
11	P1_RS232_RxD	RS-232 serial input to acq. path 1 of frame grabber (UART).
12	P1_OPTO_AUX(TRIG)_IN0+	Opto-isolated auxiliary input for acq. path 1 (positive). Supported signals: trigger input 0 (main purpose) or user input 4.
13	P2_OPTO_AUX(TRIG)_IN0+	Opto-isolated auxiliary input for acq. path 2 (positive). Supported signals: trigger input 0 (main purpose) or user input 4.
14	P2_OPTO_AUX(TRIG)_IN0-	Opto-isolated auxiliary input for acq. path 2 (negative). See pin 13 for more information.
15	LVDS/TTL_AUX(TRIG)_IN3+	LVDS/TTL auxiliary input 3 for an unspecified acq. path (positive). Signals only supported for acq. path 0: user input 7. Signals only supported for acq. path 1: field polarity input, timer clock input, user input 2, or quadrature input bit 1. Signals only supported for acq. path 2 and 3: user input 9. Signals supported for any acq. path: trigger input 3 (main purpose).
16	P0_RS232_TxD	RS-232 serial output from acq. path 0 (UART) to video source.
17	P0_OPTO_AUX(TRIG)_IN0-	Opto-isolated auxiliary input for acq. path 0 (negative). See pin 2 for more information.
18	P1_TTL_AUX(EXP)_OUT	TTL auxiliary output for acq. path 1. Supported signals: exposure output 0 (main purpose) or user output 6.
19	GND	Ground
20	LVDS/TTL_AUX(TRIG)_IN0+	LVDS/TTL auxiliary input 0 for an unspecified acq. path (positive). Signals only supported for acq. path 0: data valid input or user input 1, or quadrature input bit 0. Signals only supported for acq. path 1, 2 and 3: user input 6. Signals supported for any acq. path: trigger input 2 (main purpose).

Pin	Signal	Description
21	GND	Ground
22	LVDS/TTL_AUX(TRIG)_IN2-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary input 2 for an unspecified acq. path. See pin 7 for more information.
23	P3_OPTO_AUX(TRIG)_IN0+	Opto-isolated auxiliary input for acq. path 3 (positive). Supported signals: trigger input 0 (main purpose) or user input 4.
24	P2_TTL_AUX(EXP)_OUT	TTL auxiliary output for acq. path 2. Supported signals: exposure output 0 (main purpose) or user output 6.
25	P2_RS232_RxD	RS-232 serial input to acq. path 2 of frame grabber (UART).
26	GND	Ground
27	P1_RS232_TxD	RS-232 serial output from acq. path 1 (UART) to video source.
28	P1_OPTO_AUX(TRIG)_IN0-	Opto-isolated auxiliary input for acq. path 1 (negative). See pin 12 for more information.
29	LVDS/TTL_AUX(TRIG)_IN4-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary input 4 for an unspecified acq. path (negative). See pin 44 for more information.
30	LVDS/TTL_AUX(TRIG)_IN3-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary input 3 for an unspecified acq. path (negative). See pin 15 for more information.
31	LVDS/TTL_AUX(TRIG)_IN5-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary input 5 for an unspecified acq. path (negative). See pin 32 for more information.
32	LVDS/TTL_AUX(TRIG)_IN5+	LVDS/TTL auxiliary input 5 for an unspecified acq. path (positive). Signals only supported for acq. path 0 and 1: user input 9. Signals only supported for acq. path 2: field polarity input, timer clock input, user input 2, or quadrature input bit 1. Signals only supported for acq. path 3: user input 11. Signals supported for any acq. path: trigger input 3 (main purpose).
33	P3_TTL_AUX(EXP)_OUT	TTL auxiliary output for acq. path 3. Supported signals: exposure output 0 (main purpose) or user output 6.
34	P3_RS232_TxD	RS-232 serial output from acq. path 3 (UART) to video source.
35	P3_RS232_RxD	RS-232 serial input to acq. path 3 of frame grabber (UART).
36	GND	Ground
37	P3_OPTO_AUX(TRIG)_IN0-	Opto-isolated auxiliary input for acq. path 3 (negative). See pin 23 for more information.

Pin	Signal	Description
38	LVDS/TTL_AUX(TRIG)_IN6-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary input 6 for an unspecified acq. path (negative). See pin 39 for more information.
39	LVDS/TTL_AUX(TRIG)_IN6+	LVDS/TTL auxiliary input 6 for an unspecified acq. path (positive). Signals only supported for acq. path 0, 1, and 2: user input 10. Signals only supported for acq. path 3: data valid input, user input 1, or quadrature input bit 0. Signals supported for any acq. path: trigger input 2 (main purpose).
40	P2_RS232_TxD	RS-232 serial output from acq. path 2 (UART) to video source.
41	GND	Ground
42	LVDS/TTL_AUX(TRIG)_IN7-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary input 7 for an unspecified acq. path (negative). See pin 43 for more information.
43	LVDS/TTL_AUX(TRIG)_IN7+	LVDS/TTL auxiliary input 7 for an unspecified acq. path (positive). Signals only supported for acq. path 0, 1, and 2: user input 11. Signals only supported for acq. path 3: field polarity input, timer clock input, user input 2, or quadrature input bit 1. Signals supported for any acq. path: trigger input 3 (main purpose).
44	LVDS/TTL_AUX(TRIG)_IN4+	LVDS/TTL auxiliary input 4 for an unspecified acq. path (positive). Signals only supported for acq. path 0 and 1: user input 8. Signals only supported for acq. path 2: data valid input, user input 1, or quadrature input bit 0. Signals only supported for acq. path 3: user input 10. Signals supported for any acq. path: trigger input 2 (main purpose).

To build your own cable, you can purchase the following parts:

Manufacturer:	NorComp, Inc.
Connector:	180-044-102-001
Backshell:	970-025-010-011

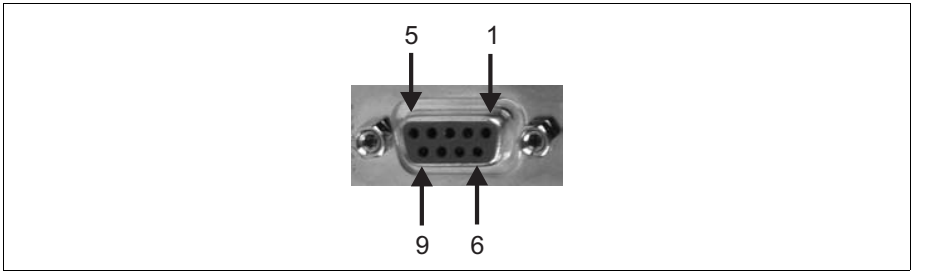
These parts can be purchased from third parties such as Digi-Key Corporation (www.digikey.com).

External auxiliary I/O connector 1

External auxiliary I/O connector 1 is a standard DB-9 female connector, located on the bracket of the cable adapter board. This connector is used to receive opto-isolated auxiliary signals; these signals can be used to route trigger or

user-defined signals. This connector interfaces with the 50-pin internal auxiliary I/O connector on the board, making the I/O signals accessible outside of the computer enclosure.

The pinout for this connector is as follows. The description of each (positive) auxiliary signal states whether the signal is specific to an acquisition path and the type of signals that can be routed onto it.



Pin	Signal	Description
1	P2_OPTO_AUX(TRIG)_IN1+	Opto-isolated auxiliary input for acq. path 2 (positive). Supported signals: trigger input 1 (main purpose) or user input 5.
2	P0_OPTO_AUX(TRIG)_IN1-	Opto-isolated auxiliary input for acq. path 0 (negative). See pin 7 for more information.
3	P3_OPTO_AUX(TRIG)_IN1-	Opto-isolated auxiliary input for acq. path 3 (negative). See pin 8 for more information.
4	P1_OPTO_AUX(TRIG)_IN1+	Opto-isolated auxiliary input for acq. path 1 (positive). Supported signals: trigger input 1 (main purpose) or user input 5.
5	P1_OPTO_AUX(TRIG)_IN1-	Opto-isolated auxiliary input for acq. path 1 (negative). See pin 4 for more information.
6	P2_OPTO_AUX(TRIG)_IN1-	Opto-isolated auxiliary input for acq. path 2 (negative). See pin 1 for more information.
7	P0_OPTO_AUX(TRIG)_IN1+	Opto-isolated auxiliary input for acq. path 0 (positive). Supported signals: trigger input 1 (main purpose) or user input 5.
8	P3_OPTO_AUX(TRIG)_IN1+	Opto-isolated auxiliary input for acq. path 3 (positive). Supported signals: trigger input 1 (main purpose) or user input 5.
9	NC	Not connected.

To build your own cable, you can purchase the following parts:

Manufacturer:	NorComp, Inc.
Connector:	172-E09-102-031
Backshell:	970-009-010-011

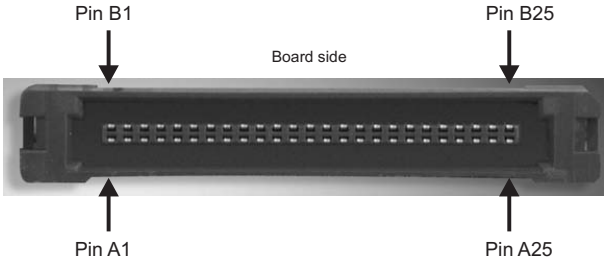
These parts can be purchased from third parties such as Digi-Key Corporation (www.digikey.com).

Internal auxiliary I/O connector

The internal auxiliary I/O connector is a 50-pin low-profile IDC connector. This connector is used to transmit/receive communication and auxiliary signals; the auxiliary signals can be used to route data valid, field, timer clock, trigger, exposure, or user-defined signals.

The connector is located on the edge of the board, making the signals accessible from inside the computer enclosure. You can use the connectors on the adapter board to access all of these signals from outside the computer enclosure.

The pinout for this connector is as follows. Refer to the description of the external auxiliary I/O connectors to establish if an auxiliary signal is specific to an acquisition path and the type of signals that can be routed onto it.



Pin	Signal	Description	Pin	Signal	Description
A1	P0_RS232_RxD	RS-232 serial input to acq. path 0 of frame grabber (UART).	B1	P0_RS232_TxD	RS-232 serial output from acq. path 0 (UART) to video source.
A2	P0_OPTO_AUX(TRIG)_IN0+	Opto-isolated auxiliary input (main purpose is trigger 0) for acq. path 0 (positive)	B2	P0_OPTO_AUX(TRIG)_IN0-	Opto-isolated auxiliary input (main purpose is trigger 0) for acq. path 0 (negative)

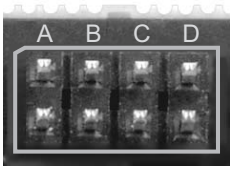
Pin	Signal	Description	Pin	Signal	Description
A3	P0_OPTO_AUX(TRIG)_IN1+	Opto-isolated auxiliary input (main purpose is trigger 1) for acq. path 0 (positive)	B3	P0_OPTO_AUX(TRIG)_IN1-	Opto-isolated auxiliary input (main purpose is trigger 1) for acq. path 0 (negative)
A4	LVDS/TTL_AUX(TRIG)_IN0+	LVDS/TTL auxiliary input 0 (main purpose is trigger 2) for an unspecified acq. path (positive).	B4	LVDS/TTL_AUX(TRIG)_IN0-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary input 0 (main purpose is trigger 2), for an unspecified acq. path (negative).
A5	GND	Ground.	B5	P0_TTL_AUX(EXP)_OUT	TTL auxiliary output (main purpose is exposure 0) for acq. path 0.
A6	LVDS/TTL_AUX(TRIG)_IN1+	LVDS/TTL auxiliary input 1 (main purpose is trigger 3) for an unspecified acq. path (positive).	B6	LVDS/TTL_AUX(TRIG)_IN1-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary input 1 (main purpose is trigger 3), for an unspecified acq. path (negative).
A7	P1_RS232_RxD	RS-232 serial input to acq. path 1 of frame grabber (UART).	B7	P1_RS232_TxD	RS-232 serial output from acq. path 1 (UART) to video source.
A8	P1_OPTO_AUX(TRIG)_IN0+	Opto-isolated auxiliary input (main purpose is trigger 0) for acq. path 1 (positive)	B8	P1_OPTO_AUX(TRIG)_IN0-	Opto-isolated auxiliary input (main purpose is trigger 0) for acq. path 1 (negative)
A9	P1_OPTO_AUX(TRIG)_IN1+	Opto-isolated auxiliary input (main purpose is trigger 1) for acq. path 1 (positive)	B9	P1_OPTO_AUX(TRIG)_IN1-	Opto-isolated auxiliary input (main purpose is trigger 1) for acq. path 1 (negative)
A10	LVDS/TTL_AUX(TRIG)_IN2+	LVDS/TTL auxiliary input 2 (main purpose is trigger 2) for an unspecified acq. path (positive).	B10	LVDS/TTL_AUX(TRIG)_IN2-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary input 2 (main purpose is trigger 2), for an unspecified acq. path (negative).
A11	GND	Ground.	B11	P1_TTL_AUX(EXP)_OUT	TTL auxiliary output (main purpose is exposure 0) for acq. path 1
A12	LVDS/TTL_AUX(TRIG)_IN3+	LVDS/TTL auxiliary input 3 (main purpose is trigger 3) for an unspecified acq. path (positive).	B12	LVDS/TTL_AUX(TRIG)_IN3-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary input 3 (main purpose is trigger 3), for an unspecified acq. path (negative).
A13	GND	Ground.	B13	GND	Ground.

Pin	Signal	Description	Pin	Signal	Description
A14	P2_RS232_RxD	RS-232 serial input to acq. path 2 of frame grabber (UART).	B14	P2_RS232_TxD	RS-232 serial output from acq. path 2 (UART) to video source.
A15	P2_OPTO_AUX(TRIG)_IN0+	Opto-isolated auxiliary input (main purpose is trigger 0) for acq. path 2 (positive)	B15	P2_OPTO_AUX(TRIG)_IN0-	Opto-isolated auxiliary input (main purpose is trigger 0) for acq. path 2 (negative)
A16	P2_OPTO_AUX(TRIG)_IN1+	Opto-isolated auxiliary input (main purpose is trigger 1) for acq. path 2 (positive)	B16	P2_OPTO_AUX(TRIG)_IN1-	Opto-isolated auxiliary input (main purpose is trigger 1) for acq. path 2 (negative)
A17	LVDS/TTL_AUX(TRIG)_IN4+	LVDS/TTL auxiliary input 4 (main purpose is trigger 2) for an unspecified acq. path (positive).	B17	LVDS/TTL_AUX(TRIG)_IN4-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary input 4 (main purpose is trigger 2), for an unspecified acq. path (negative).
A18	GND	Ground.	B18	P2_TTL_AUX(EXP)_OUT	TTL auxiliary output (main purpose is exposure 0) for acq. path 2.
A19	LVDS/TTL_AUX(TRIG)_IN5+	LVDS/TTL auxiliary input 5 (main purpose is trigger 3) for an unspecified acq. path (positive).	B19	LVDS/TTL_AUX(TRIG)_IN5-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary input 5 (main purpose is trigger 3), for an unspecified acq. path (negative).
A20	P3_RS232_RxD	RS-232 serial input to acq. path 3 of frame grabber (UART).	B20	P3_RS232_TxD	RS-232 serial output from acq. path 3 (UART) to video source.
A21	P3_OPTO_AUX(TRIG)_IN0+	Opto-isolated auxiliary input (main purpose is trigger 0) for acq. path 3 (positive)	B21	P3_OPTO_AUX(TRIG)_IN0-	Opto-isolated auxiliary input (main purpose is trigger 0) for acq. path 3 (negative)
A22	P3_OPTO_AUX(TRIG)_IN1+	Opto-isolated auxiliary input (main purpose is trigger 1) for acq. path 3 (positive)	B22	P3_OPTO_AUX(TRIG)_IN1-	Opto-isolated auxiliary input (main purpose is trigger 1) for acq. path 3 (negative)
A23	LVDS/TTL_AUX(TRIG)_IN6+	LVDS/TTL auxiliary input 6 (main purpose is trigger 2) for an unspecified acq. path (positive).	B23	LVDS/TTL_AUX(TRIG)_IN6-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary input 6 (main purpose is trigger 2), for an unspecified acq. path (negative).
A24	GND	Ground.	B24	P3_TTL_AUX(EXP)_OUT	TTL auxiliary output (main purpose is exposure 0) for acq. path 3

Pin	Signal	Description	Pin	Signal	Description
A25	LVDS/TTL_AUX(TRIG)_IN7+	LVDS/TTL auxiliary input 7 (main purpose is trigger 3) for an unspecified acq. path (positive).	B25	LVDS/TTL_AUX(TRIG)_IN7-	Negative component when LVDS signal arriving on LVDS/TTL auxiliary input 7 (main purpose is trigger 3), for an unspecified acq. path (negative).

System reset connector

Matrox Helios XD has a system reset connector. The system reset connector is a standard, 0.1" spacing, 8-pin male connector, used to reset the motherboard if the reset button is pressed or the Watchdog circuitry of Matrox Helios detects abnormal Host inactivity. The system reset connector's pin assignment is as follows. Note that it does not matter which pin in the pair is pin 1.



Matrox Helios XD

Pin pair	Pin	Signal	Description
A	1	RESET_MB	Reset signal output (usually to motherboard).
	2	GND_MB	Motherboard active reset level (usually ground).
B	1	RESET_BUTTON	Reset signal input (usually from Reset button).
	2	GND_MB	Motherboard active reset level (usually ground).
C	1 and 2	-	Reserved.
D	1 and 2	-	Reserved.

To build your own cable, parts can be purchased from:

Manufacturer	FCI
Crimp-to-wire receptacle	76357-301 (discrete contact; wire size: 22-30 AWG)
Housing	65039-035 (2 positions)

Ventilation requirements

This section describes how to determine the ventilation requirements for a Matrox Helios system enclosure. Ventilation moderates the steady-state internal temperature rise in the enclosure; the sum of the temperature rise and the room operating temperature should not exceed the maximum operating temperature supported by Matrox Helios. Note that the figures mentioned assume near sea level atmospheric pressure and a room operating temperature near 25°C.

This section is only an introduction to thermal management; you can refer to the web site of a fan manufacturer for more detailed information on this subject. For example, you can refer to the engineering information provided on the site of the Sunonwealth Electric Machine Industry Company (www.sunon.com.tw).

Basic equation

The basic equation to determine how much air flow is required in the enclosure is as follows:

```
Q(cfm) = 1.76 x P/dTc
Q(m3/min) = 0.05 x P/dTc


Q:  Required air flow (m3/min or cfm (cubic feet per minute))
P:  Internal heat dissipation (W)
dTc: Internal temperature rise (°C)
```

The enclosure size does not influence steady-state internal temperature rise; it only affects the dynamic character of the rise. A larger enclosure takes more time to attain a steady state.

To properly select a fan for your enclosure, you must estimate the pressure build-up in your enclosure. To do so, you need to estimate the relationship between the fan size, the opening of the enclosure on the intake side, and the opening of the enclosure on the exhaust side.

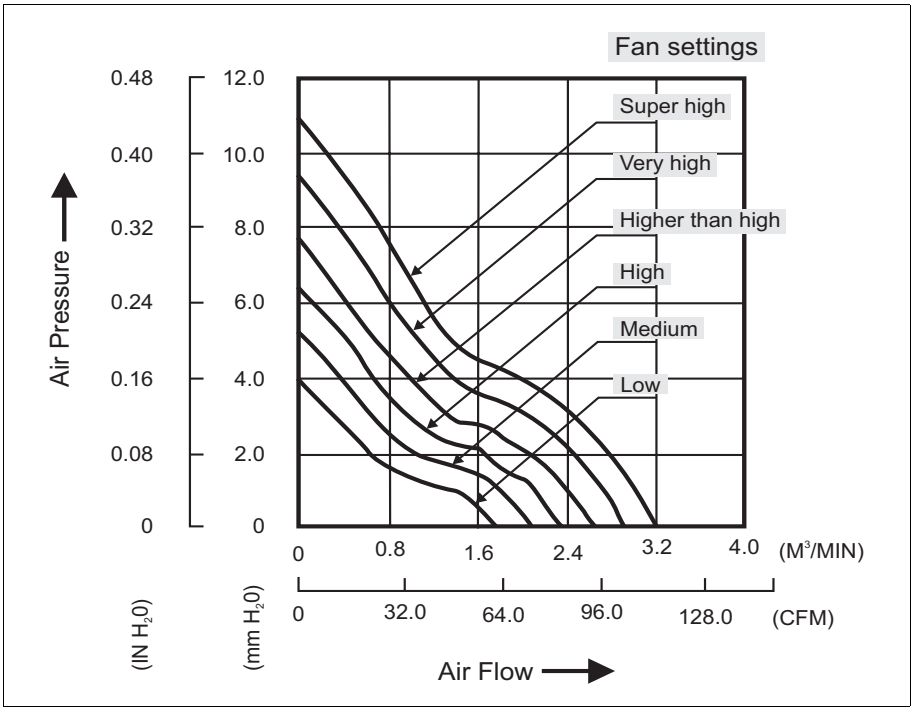
If your intake and exhaust opening is bigger than the fan area, your enclosure should not build any pressure. Due to turbulence, cabling, and direction change of the air flow in the enclosure, there is always some pressure build-up, even if the intake and exhaust openings are sufficient. A typical desktop computer enclosure builds up around 3.75 mm of H_2O of pressure.

If the enclosure has smaller openings than the fan area, you must add this resistance to the enclosure pressure. If you have a 80 mm x 80 mm fan and only the equivalent of a 60 mm x 60 mm enclosure opening, you have an area ratio of (60 x 60)/(80 x 80) =3600/6400 = 0.5625. So your fan will already be at 56% of its maximum supported pressure. You must add this value to the turbulent contribution of the enclosure.

With this information, you can now select a fan. If you decide that you need more than one fan, putting them in parallel will double the flow. Putting them in series (one intake and one exhaust or two stacked intakes/exhausts) will double the pressure.

Fan example

The following provides an example of how to calculate the amount of air flow required. It uses an enclosure in which you are dissipating 300 W. In addition, it uses a typical 120 mm x 120 mm x 25 mm 12 V fan that is operating at high speed. Note that very high speeds are not recommended because they significantly reduce the life of the fan.



In this case, the opening of the intake and exhaust has the same area as that of the fan (14400 mm^2). This means that you only have to deal with the turbulent pressure.

A single fan at 3.75 mm of H_2O of pressure results in about 0.66 m^3/min of air flow. Using the previously mentioned formula, you get

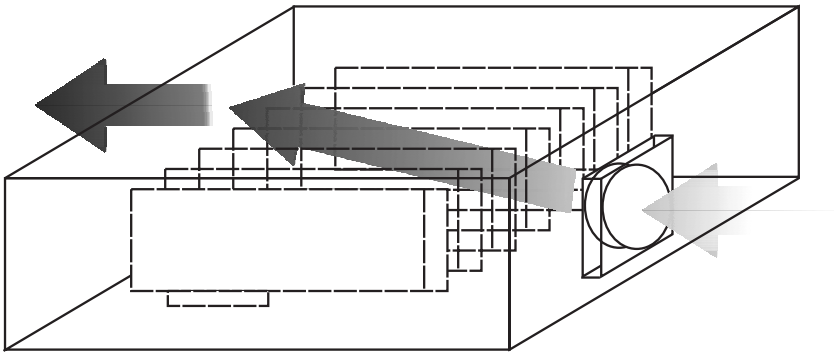
dTc=0.05 x P/Q

dTc=0.05 x 300/0.66

dTc= 22.7°C of rise in the enclosure.

Optimal placement

Optimally, the fans will be placed in front of the PCI/PCI-X boards, as illustrated in the following diagram, to increase the airflow between boards and prevent hot spots:



Flow/pressure charts

Refer to your fan's data sheet for flow/pressure charts (available from fan manufacturer). If you use fans in series, you must stretch their chart vertically by 2. If you use fans in parallel, you must stretch their chart horizontally by 2. By doing so, it becomes clear that if for a certain pressure, a fan gives 0 air flow, adding a fan, even in parallel, does not help.

Appendix C: Listing of Matrox Helios boards

This appendix lists specific versions and revisions of the Matrox Helios board.

Revisions of Matrox Helios

Board	PCB Version	*Description*
Matrox Helios XCL dual-Base	7108-00 rev. A	• Original version. • 3.3 V PCI tolerant.
	7108-01 rev. A	• 3.3 V / 5 V PCI tolerant. • Support for Watchdog.
Matrox Helios XCL single-Full	7108-00 rev. A	• Original version. • 3.3 V PCI tolerant.
	7108-01 rev. A	• 3.3 V / 5 V PCI tolerant. • Support for Watchdog.
Matrox Helios XA	7157-00 rev. B	• Original version. • 3.3 V PCI tolerant.
	7157-01 rev. A	• 3.3 V / 5 V PCI tolerant.

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Regulatory compliance for Matrox Helios XA

FCC Compliance Statement

Warning

Changes or modifications to this unit not expressly approved by the party responsible for the compliance could void the user's authority to operate this equipment.

Note

This device complies with Part 15 of FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this device in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his/her own expense. The user is advised that any equipment changes or modifications not expressly approved by the party responsible for compliance would void the compliance to FCC regulations and therefore, the user's authority to operate the equipment.

Industry Canada Compliance Statement

This digital apparatus does not exceed the Class A limits for radio noise emission from digital apparatus set out in the Radio Interference Regulations of Industry Canada.

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de Classe A prescrites dans le Règlement sur le brouillage radioélectrique édicté par Industrie Canada.

EU Notice (European Union)

WARNING: This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

AVERTISSEMENT: Cet appareil est de la classe A. Lorsque cet appareil est utilisé dans un environnment résidentiel, il peut entraîner des interférences radioélectriques. Dans ce cas, l'usager peut être prié de prendre des mesures correctives appropriées.

This device complies with EC Directive 89/336/EEC for a Class A digital device. It has been tested and found to comply with EN55022/CISPR22 and EN55024/CISPR24 when installed in a typical class A compliant host system. It is assumed that this device will also achieve compliance in any Class A compliant system.

Le présent appareil numérique répond aux exigences stipulées dans la directive européenne 89/336/EEC prescrite pour les appareils numériques de classe A. Ce produit a été testé conformément aux procédures EN55022/CISPR22 et EN55024/CISPR24 dans un système hôte typique et conforme à la classe A. On peut présumer que cet appareil sera aussi conforme s'il est utilisé dans n'importe quel système de classe A.

Regulatory compliance for Matrox Helios XCL and XD

FCC Compliance Statement

Remark for the Matrox hardware products supported by this guide

These devices have been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures: • Reorient or relocate the receiving antenna • Increase the separation between the equipment and receiver • Connect the equipment into an outlet on a circuit different from that to which the receiver is connected • Consult the dealer or an experienced radio/TV technician for help.

WARNING

Changes or modifications to this unit not expressly approved by the party responsible for the compliance could void the user's authority to operate this equipment. The use of shielded cables for connection of the monitor to the card is required to meet FCC requirements.

Declaration of conformity of a Class B digital device according to the FCC rules

We, the Responsible Party

Matrox International Corporation, 625 State Route 3, Unit B, Plattsburg, NY 12901-6530
Telephone: (514) 822-6000 (x2026) • Attention: Conformity Group

Declaration

The Matrox hardware products supported by this guide comply with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) these devices may not cause harmful interference, and (2) these devices must accept any interference received, including interference that may cause undesired operation. Any question regarding this declaration should be forwarded to the above coordinates.

(English) Industry Canada Compliance Statement

Remark for the Matrox hardware products supported by this guide

These digital devices do not exceed the Class B limits for radio noise emission from digital apparatus devices set out in the Radio Interference Regulation of Industry Canada.

(Français) Conformité avec les exigences du ministère de l'Industrie Canada

Remarque sur les produits matériels Matrox couverts par ce guide

Ces appareils numériques n'émettent aucun bruit radioélectrique dépassant les limites applicables aux appareils numériques de Classe B prescrites dans le Règlement sur le brouillage radioélectrique édicté par Industrie Canada.

(English) European user's information – Declaration of Conformity

Remark for the Matrox hardware products supported by this guide

These devices comply with EC Directive 89/336/EEC for a Class B digital device. They have been tested and found to comply with EN55022/CISPR22 and EN55024/CISPR24. In a domestic environment these products may cause radio interference in which case the user may be required to take adequate measures.To meet EC requirements, shielded cables must be used to connect the monitor and other peripherals to the card. These products have been tested in a typical class B compliant host system. It is assumed that these products will also achieve compliance in any class B compliant system.

(Français) Informations aux utilisateurs Européens – Déclaration de conformité

Remarque sur les produits matériels Matrox couverts par ce guide

Ces unités sont conformes à la directive communautaire 89/336/EEC pour les unités numériques de classe B. Les tests effectués ont prouvé qu'elles sont conformes aux normes EN55022/CISPR22 et EN55024/CISPR24. Le fonctionnement de ces produits dans un environnement résidentiel peut causer des interférences radio, dans ce cas l'utilisateur peut être amené à prendre les mesures appropriées. Pour respecter les impératifs communautaires, les câbles de connexion entre le moniteur ou autres périphériques et la carte doivent être blindés. Ces produits ont été testés dans un système hôte typique compatible classe B. On suppose qu'ils présenteront la même compatibilité dans tout système compatible classe B.

(Deutsch) Information für europäische Anwender – Konformitätserklärung

Anmerkung für die Matrox Hardware-Produktunterstützung durch dieses Handbuch

Diese Geräte entsprechen EC Direktive 89/336/EEC für ein digitales Gerät Klasse B. Sie wurden getestet und entsprechen demnach EN55022/CISPR22 und EN55024/CISPR24. In einer Wohnumgebung können diese Produkte Funkinterferenzen erzeugen, und der Benutzer kann genötigt sein, entsprechende Maßnahmen zu ergreifen. Um EG-Anforderungen zu entsprechen, müssen zum Anschließen des Monitors und anderer Peripheriegeräte an die Karte abgeschirmte Kabel verwendet werden. Diese Produkt wurden in einem typischen, der Klasse B entsprechenden, Host-System getestet. Es wird davon ausgegangen, daß diese Produkte auch in jedem Klasse B entsprechenden System entsprechend funktionieren.

(Italiano) Informazioni per gli utenti europei – Dichiarazione di conformità

Nota per i prodotti hardware Matrox supportati da questa guida

Questi dispositivi sono conformi alla direttiva CEE 89/336/EEC relativamente ai dispositivi digitali di Classe B. Sono stati provati e sono risultati conformi alle norme EN55022/CISPR22 e EN55024/CISPR24. In un ambiente domestico, questi prodotti possono causare radiointerferenze, nel qual caso all'utente potrebbe venire richiesto di prendere le misure adeguate. Per soddisfare i requisiti CEE, il monitor e le altre periferiche vanno collegati alla scheda grafica con cavi schermati. Questi prodotti sono stati provati in un tipico sistema host conforme alla classe B. Inoltre, si dà per scontato che questi prodotti acquisiranno la conformità in qualsiasi sistema conforme alla classe B.

(Español) Información para usuarios europeos – Declaración de conformidad

Observación referente a los productos de hardware de Matrox apoyados por este manual

Estos dispositivos cumplen con la directiva de la CE 89/336/EEC para dispositivos digitales de Clase B. Dichos dispositivos han sido sometidos a prueba y se ha comprobado que cumplen con las normas EN55022/CISPR22 y EN55024/CISPR24. En entornos residenciales, estos productos pueden causar interferencias en las comunicaciones por radio; en tal caso el usuario deberá adoptar las medidas adecuadas. Para satisfacer las disposiciones de la CE, deberán utilizarse cables apantallados para conectar el monitor y demás periféricos a la tarjeta. Estos productos han sido sometidos a prueba en un típico sistema anfitrión que responde a los requisitos de la clase B. Se supone que estos productos cumplirán también con las normas en cualquier sistema que responda a los requisitos de la clase B.

Product support

Limited Warranty

Matrox warrants this product against defects in materials and workmanship for a period of ***one year*** *from the date of delivery. Matrox and its suppliers expressly disclaim any and all other warranties, express or implied.*

Your sole remedy shall be, repair or replacement of the product provided that the defective product be returned to the authorized dealer within a year from the date of delivery.

If you wish to return your board, contact the Matrox authorized dealer where you purchased the board for service. ***Do not return a product to Matrox without authorization****.*

In the event you must return the board directly to Matrox, follow these steps:

1. Contact Customer Support (The *Customer support contacts* information sheet included in your package has the phone numbers for Matrox's offices).

   Customer Support will ask you to describe the problem and will issue a Return Merchandise Authorization (RMA).

2. Leave the configuration as it was when you were using the board.
3. Pack the board in its original box and return it with a completed "Product Assistance Request" form (provided in the following page).

Return address

U.S. customers must return their products to our U.S. address:

- Matrox International Corp.
  625 State Route 3, Unit 1
  Plattsburgh, N.Y.
  12901

Canadian and other international customers can return their products directly to our Canadian facility:

- Matrox Electronic Systems Ltd.
  1055 St. Regis Blvd.
  Dorval, Quebec
  H9P 2T4

Product Assistance Request Form

Name:	
Company:	
Address:	
Phone:	Fax:
E-mail:	
Hardware Specific Information	
Computer:	CPU:
System memory:	PCI Chipset:
System BIOS rev:	
Video card used:	Resolution:
Network Card:	Network Software:
Other cards in system:	
Software Specific Information	
Operating system:	Rev:
Matrox SW used:	Rev:
Compiler:	Rev:
Fill out only if you are returning a board	
RMA #:	
Who were you talking to in customer support?	
Date board was received:	Date of failure:
MOD #:	These numbers are on the label at the back of the board.
SER #:	
REV #:	
PMB #:	
PNS #:	
Can you reproduce the problem? Yes ❒ No ❒	
Is an error code displayed? Yes ❒ No ❒	If so, what code?
	... Continued on reverse

Describe the problem: